Low Temperature Performance of COTS Electronic Components for Martian Surface Applications

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Abstract—Commercial-off-the-shelf (COTS) components were tested over the Martian temperature range for their use in a MARS proximity microtransceiver development project. These COTS components include off-chip IF filters, off-chip TCXOs, and on-chip components such as MOSFETS, resistors and capacitors. The on-chip components are from a rad-hard Silicon-on-Sapphire (SOS) IC process. Novel methods were developed to reliably measure component characteristics at cryogenic temperatures. Measurements were then taken from 25°C to -120°C in steps of 20°C. The results achieved look promising and provide useful information for analog circuit designers developing circuitry for extreme low temperature ranges.

Figure 1. Simplified block diagram of the transceiver chip [5].

I. INTRODUCTION

Electronic Components that are capable of operating at cryogenic temperatures will be required for many future NASA space missions including the joint K-State / JPL / Peregrine Semiconductor Mars Proximity Microtransceiver project. Operating at low temperatures without the typical "warm box" used on current missions promises to help reduce payload development and launch cost in addition to survive harsh deep space environments. A major goal in the initial part of the project was to characterize the low temperature behavior of the basic SOS process from Peregrine Semiconductor and commercially available filters and TCXOs (Temperature Compensated Crystal Oscillators). In this research computer-controlled equipment was developed which interfaced with a Sigma Systems temperature controller, power supplies and multi meter using IEEE GPIB- 488 standard for data acquisition. Measurements were then taken on the TCXOs, filters, and Peregrine wafer process control monitor (PCM) structures and the data was formatted for easy use by circuit designers who will participate in the project later.

The COTS components used in the transceiver design are shown in Figure-1. This paper will discuss the methods used for testing the COTS components and the results obtained. A companion paper discusses the transceiver architecture and the use of COTS components for its design.
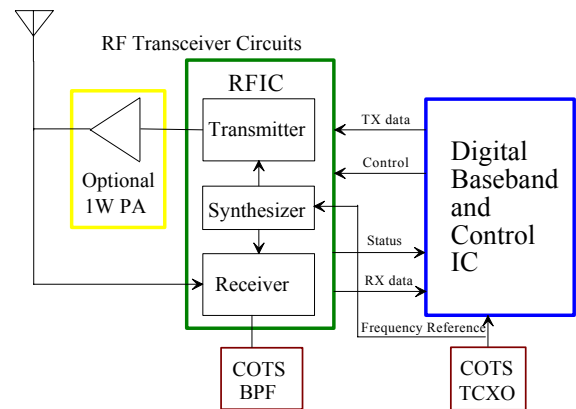
II. COMPONENTS OF CRYOGENIC TESTING

Cryogenic cooling is a process of bringing down the temperature of the DUT (Device under Test) by using coolants such as liquid nitrogen and liquid carbon dioxide. A liquid absorbs heat while going to vapor state and thus the idea behind cryogenic cooling is to make a liquid vaporize and thus cool the DUT by removing heat from its surroundings.

In the current project, to cool the aluminum platform and the DUT attached to it, a pressurized liquid has to be introduced from a pressure-building tank through a throttling device. The throttle valve reduces the pressure of the liquid to vaporize it, thus taking away heat from the platform. In order to control the cooling rate, the amount of liquid being vaporized needs to be controlled. This is done with the help of a temperature controller, which uses a closed loop system to sense the temperature and open/close a solenoid valve. To achieve higher temperatures the temperature controller also has heating coils. The temperature controller controls the temperature of the platform by either controlling the flow of the liquid coolant or by allowing the coils to heat up, which are just beneath the temperature platform.

As the area of interest is in testing the electronic components at or around the temperature that exists on Mars, a thermal platform is used, the temperature of which could reduce to a minimum of -120° C or increase to a maximum of 200° C (The highest temperature reported from summer 2004 on the Mars was only -20°C). The other requirement for the

cryogenic cooling of the electronic components is that the conductivity between the DUT and the thermal platform should be fast enough to stabilize them quickly to speed up the process and hence save coolant.
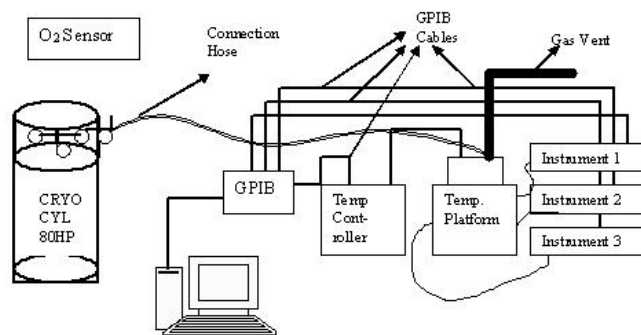

Figure-2 Components of K-State cryogenic test bench

The coolant is stored in a pressure building dewar which is connected to a thermal platform with a high pressure hose. The amount of liquid coolant entering the thermal platform is controlled with a temperature controller, which varies the amount of liquid coolant with a metering valve and a throttling injector. The DUT is kept on the thermal platform and is connected to various measuring and controlling instruments. The system contains a permanent 500Ω RTD type temperature probe mounted just inside the thermal platform. An optional similar probe is attached to the DUT for better control of temperature. For the current research, we use this probe to assure accurate temperature at the DUT. The temperature controller together with all the other instruments is connected through GPIB to a workstation running LabVIEW, measurement and control software. LABVIEW program controls most of the instruments. Automated tests can be programmed for testing MOSFET characteristic curves.

III. EXPERIMENTAL SETUP

The main concerns in the COTS cryogenic testing included setting up the correct temperature of DUT, minimizing frost accumulation (on test boards and on semiconductor wafer) and avoiding thermal conduction between wires running from the measuring instruments to the test boards.

The DUT and the platform are joined by a thermal compound, which helps the DUT to remain in good thermal contact with the platform. The optional temperature probe is attached close to the component test area on to the DUT. It is then held constant on that spot using a thermal compound. Temperature Controller uses an advanced algorithm, known as T-Drive, to control the temperature using both the probes.

The polycarbonate cover, used for covering the platform from external air when testing board level devices has a purge gas inlet, which can be used to introduce dry nitrogen inside. To ensure no frost accumulation when the platform is ramped to lower temperature, a polycarbonate cover is used over the

thermal platform. This cover has a purge gas inlet which is used to introduce dry nitrogen. The purge gas maintains a positive pressure of nitrogen as compared to outside air and thus doesn't allow the external air to enter the platform. While Filters and TCXOs can be tested using this setup, testing MOSFETs require probes to be positioned on the semiconductor wafer and thus both can't be tested in the same way since we cannot use the polycarbonate cover. Hence a high-pressure purge gas was used to avoid frost building up just close to the test area on to the wafer. The experimental setup for both these categories of COTS components are discussed below.

A. *Filters and TCXOs*

COTS filters and TCXOs that meet the required specifications of the current design were selected and mounted on FR4 substrate circuit boards. These components were carefully soldered along with the surface mount resistors and capacitors using reflow soldering and care was taken to ensure that the solder uniformly filled the gap between the contact surface and the component so as to protect the solder joints from breaking at low temperature. For I/O and voltage supply, 28 AWG plastic insulated wires with 2 pin connectors were used. A total of 10 COTS electronic components including 5 filters and 5 TCXO were fabricated on FR4 substrate circuit board as shown in Figure 3.
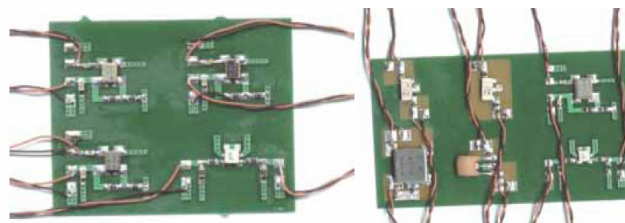

Figure-3 COTS Filters and TCXOs on circuit board

To maintain a more uniform temperature on all sides of the test board, it was decided to build a mini-chamber, made of aluminum as shown in figure 4. Thermal platforms are made of ground 6061-T6 aluminum and thus a thermal housing built from aluminum can be screwed on top of this. Moreover 6061-aluminum is weldable and thus a mini-chamber (house type structure) can be made on the thermal platform's aluminum plate. This mini-chamber has holes of 9/16 inches diameter on its two sides for the I/O wires, which can be plugged airtight when not used. One of the holes on the mini-chamber can be used as a purge gas entry port for a case when more than 2 holes are used for the I/O wires. The thickness of each side of the mini-chamber including the roof is same as the aluminum plate promoting good thermal conduction to maintain the temperature on all six inside walls. The height of the side walls is kept to 1.5 inches. The plate was metal blasted to give it a completely flat finish and also to prevent any corrosion.
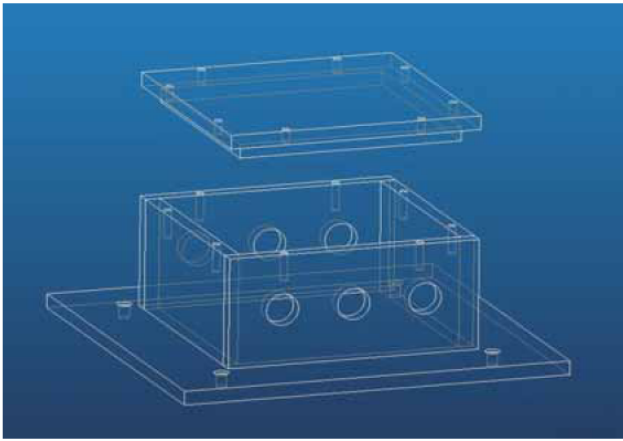
Figure 4 – Mini Chamber for testing Filters and TCXOs

The roof is the only removable part of this assembly, which can be fitted to the walls of the mini-chamber with 8 screws to make good thermal contact. This complete assembly can be fixed on top of the thermal platform.

While testing, a thermal compound is applied to the floor of the mini-chamber and then the circuit board is lowered into this on top of a thermal compound. A small amount of thermal compound is then placed on the circuit board and the DUT temperature measuring probe is then placed on this thermal compound with some small object on top of the probe so that enough pressure is applied on it to make sure that it is pressed hard enough on the circuit board and doesn't move while testing. A small block of black sponge just the size of the mini-chamber is kept on the circuit board and the roof is then lowered and screwed carefully. The complete process is shown in Figure 5 through Figure 8.
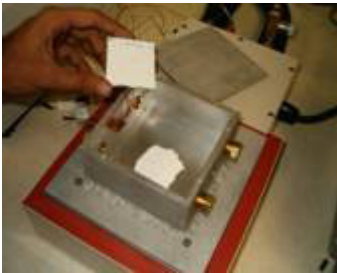

Figure 5. Step-1 Thermal compound is applied to the aluminum plate and bottom of the circuit board.

Figure 6. Step-2 DUT temperature sensing probe is placed in the center of the circuit board over thermal compound

Figure 7. Step-3 A block of black sponge is lowered carefully which is pressed with a little pressure when the roof is screwed.

Figure 8. Step-4 DUT along with the thermal platform is then covered with a polycarbonate cover. Foam plugs seal the enclosure to allow building of positive pressure of dry nitrogen.

After the circuit board is carefully placed in the mini-chamber, the unused holes are plugged with metallic compression fitting plugs. The whole platform is then covered with a polycarbonate cover as shown below which has a dry nitrogen purge gas inlet and has small opening on its two sides. The wires (not shown in the figure) are brought out from these openings and then these openings are filled with a special type of sponge to prevent the air entering in to the platform.

During the test, at a particular temperature, measurements are taken from all the components. The wires coming out of the thermal platform have corresponding labels for its type (input/output) and component. These wires connect to proper terminal/calibration boards from where the cables can be connected to the spectrum/network analyzer or power supply. Before a test, measuring instruments are warmed up for about fifteen minutes to get optimized readings

B. *Semiconductor Wafer*

The mini-chamber used for testing the filter/TCXO circuit board cannot be used for the semiconductor wafer since the components fabricated on this wafer are microscopic (50 micron a the probe tip) in size and require needle probes to be positioned on them. The probe positioners, because of their shape, do not allow any polycarbonate cover on top. These probes also need to be monitored during a test because a small movement can cause them to move off the terminal of the measured component. Moreover the delicate nature of the wafer doesn't allow anything except probe tip and temperature measuring probe to be put on top of it.

The thermal platform accumulates a lot of frost if this wafer is kept exposed to the air. A novel solution was found out to overcome the above problem. In order to prevent the air and frost accumulation reaching the small portion of the test area on the wafer a high-pressure dry nitrogen purge just above the test spot on the wafer was used (Fig.11). This dry nitrogen purge was released carefully from a tube mounted on a probe positioner, which is positioned very close to the test spot over the testing probe. After doing several runs on a wafer it was found out that the purge gas tube should be

placed 0.5 cm over and 1.0 cm away from the measuring probe for a no frost condition on the test spot.

To perform testing of the components, the semiconductor wafer is placed directly on to the thermal platform with thermal compound in between the two surfaces. The temperature measuring probe is then placed on top of this wafer with thermal compound between the surfaces. The signal measuring probes are then positioned on the right terminal of the measured component on the semiconductor wafer with the help of a microscope. These probes positioners are placed on two elevated flat objects. To make sure that they don't move during a test, vacuum is created between the flat object and the bottom of the positioners surface. Pictures in Figure 9-12 show the above process:
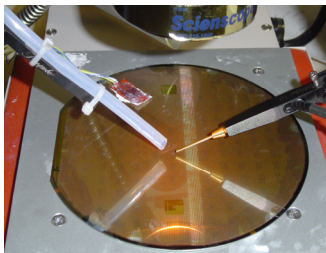

Figure 9. Semiconductor Wafer placed on the temperature platform. Purge gas tube (L), measuring probe (R). Temperature measuring probe is stacked on to the wafer
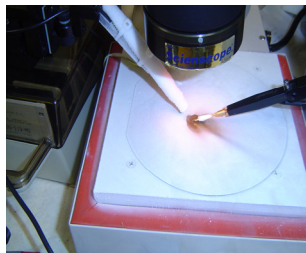

Figure 10. Semiconductor Wafer at -110C (The small test area in the center remains frost free).
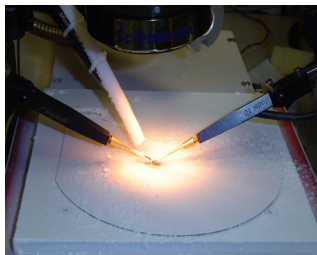

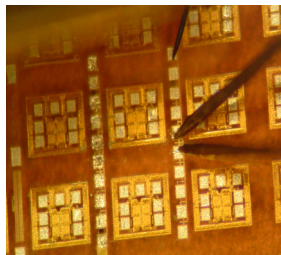Figure 11. Picture showing the case of two measuring probes used at -110C.

Figure 12. Picture taken from a microscope shows the test area magnified. The probe is placed on three terminals of a FET.

The above method works even for two measuring-probe tests setup such as when testing a FET. Fig 28 shows a magnified region of the test area as seen from microscope. To verify that the purge gas does not affect the temperature of the semiconductor device being measured, the purge gas was momentarily shut off and the measured spot was allowed to frost over. No variation in measured value was detected, indicating that the device temperature did not change. Note

that in general, however, the purge gas cannot be interrupted during measurement because the spot must remain clear to allow periodic probe tip position correction as cooling takes place.

IV. RESULTS

A. *TCXOs*

Five different COTS TCXOs (CTS OSC1606A, CTS OSC1645A, Citizen CSX532T, ECS VC-TXO-35SM, ECS VC-TXO-39SM) were chosen for testing purposes. The nominal frequencies of these TCXOs were 19.2MHz and 19.44MHz. Appropriate supply voltages were applied and the output signal was monitored on a spectrum analyzer. The main focus of this test was to know the frequency shift at lower temperatures and to determine parts per million (PPM) shift in frequency. The TCXO will be used as reference frequency generator in a Phased Lock Loop (PLL) to produce a desired frequency of 400 MHz. The Mars transceiver project uses 400 MHz frequency band for transmission and reception of radio signal and hence the change in the reference frequency will be converted to change at this frequency level. The plot in Figure 15 shows the frequency variation at 400 MHz. The shift on the y-axis corresponds to the change in frequency from room temperature. Thus at very low temperatures there will be considerable frequency change reflected at the output of the PLL.

The results from the cryogenic test of above TCXOs are presented in Figure 13 - 17. As seen on the graph on Figure-13, results down to -40˚C are in compliance with the published data but frequency stability decreases drastically after -40˚C due to the TCXO inability to shift the crystal's frequency sufficiently.
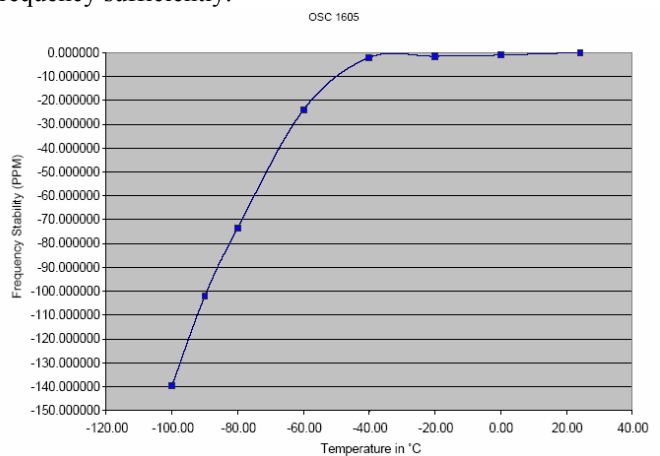

Figure 13. Plot showing frequency stability Vs Temperature for OSC 1605

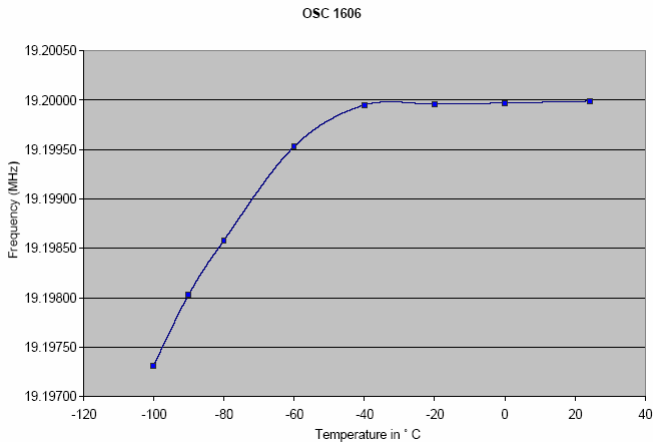The next plot shows the actual change in frequency with temperature.

Figure 14. Frequency shift at the output of PLL Vs Temperature

The plot in Figure 16 shows the signal strength at the nominal frequency for various temperatures. The signal strength is quite stable and decreases a little from the room temperature. It is measured with a 10 KΩ load resistor.
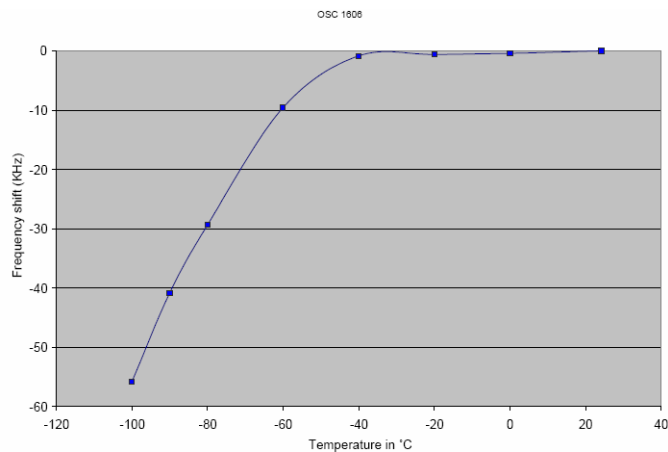

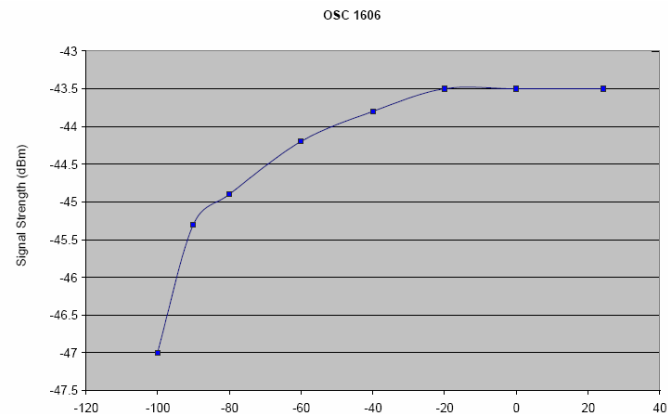Figure 15. Frequency shift at the output of PLL Vs Temperature

Figure 16. Plot for Signal Strength Vs Temperature for OSC 1606

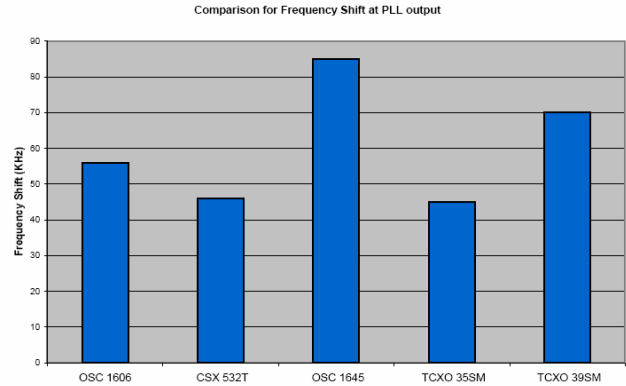A comparison of frequency shift at the PLL output for all the TCXOs is shown in Figure-17.

Figure 17. Comparison of TCXOs for the frequency shift for -100°C at PLL output

B. *Ceramic Filters*

Ceramic filters are used to isolate the desired signal at the Intermediate Frequency (IF) after the downconversion in the receiver and prior to digital demodulation. A variety of 10.7 MHz COTS ceramic filters from muRata were tested (SFELA10M7EA00-B0, SFECS10M7DF0021-R0, SFECS10M7FA00-R0, SFECV10M7CQ0C01-R0, and SFECV10M7JA00-R0). Measurements were made from 8.2 to 13.2 MHz with series resistors at the input and output (typically 300 Ω except 470 Ω for one of the filter) to provide proper termination for the input/output impedance after connecting to 50 Ω test equipment. These resistors are mounted on the test board and then connected to test equipment using twisted-pair wires for low heat conduction from the board. An HP 8753 network analyzer was used for measuring S21 parameter at various temperatures with the losses of the terminating resistors calibrated out.

All filters showed good stability in shape, center frequency, and spurious responses. All shifted downward with frequency, roughly tracking the TCXO shifts. Also the maximum shift is less than half the bandwidth of the filters (~100-150 KHz).
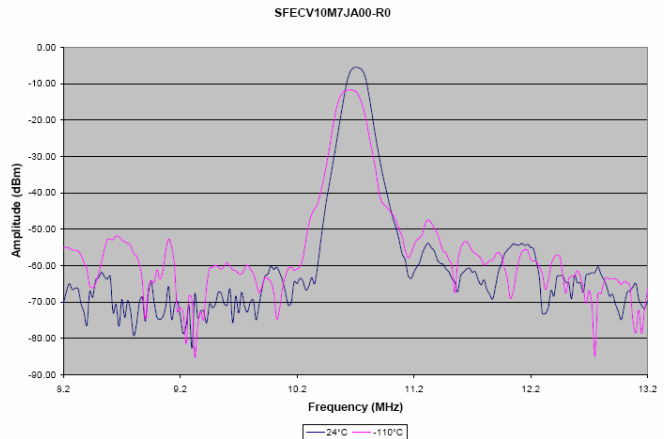

Figure 18. Frequency Response of the ceramic filter JA00 at room temperature and at -110°C.
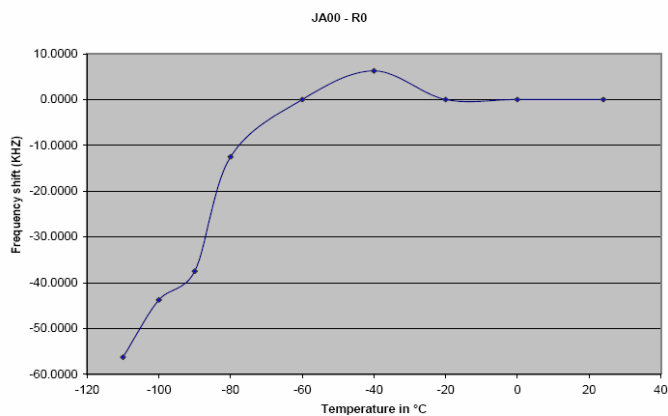
Figure 19. Frequency shift Vs Temperature for ceramic filter JA00-R0

As seen from the graph above the filter shifts downward in frequency at low temperatures and the gain decreases with decrease in temperature.. It is seen that shift in frequency increases more rapidly as we go below -100˚C.
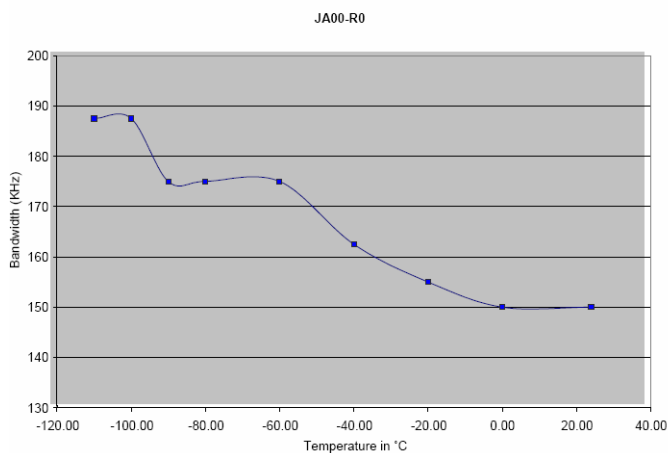

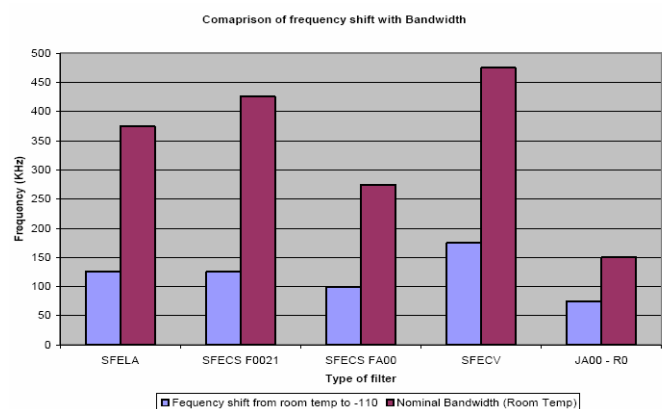Figure 20. Bandwidth Vs Temperature for ceramic filter JA00-R0

Figure 21. Comparison of frequency shift (from 24˚C to -110˚C) with Bandwidth (24˚C)

C. *Resistors*

As discussed previously the resistors tested here are various types of commercial fabricated resistors on a Peregrine wafer. A wafer containing resistors of different types with various width/length (W/L) ratios was provided from Peregrine Semiconductor. The test data here refers to the tests done on different type of this 20/80 size resistor. The different resistors provided on this wafer are P+, N+, Polycide, SN, Poly RN, Poly RP and PL type. These resistors differ from one another by the type of material used and the extent of doping. Table no. 1 summarizes the actual reading with temperature as recorded on Agilent 34401A multimeter. Resistors P+, N+, Polycide, Poly RN, Poly RP and PL have positive temperature coefficient and there resistance decreases at low temperatures while resistor SN has a negative temperature coefficient and its resistance increases at low temperatures.

Tempe-rature ˚C	Polycide	SN (KΩ)	P+ KΩ	N+ Ω	Poly RN Ω	Poly RP Ω	PL M Ω
24	47.6	7.913	.8910	625	48	64.2	1.2465
-1.9	46.7	8.244	.8499	613	48.9	63.7	1.3560
-22.7	46.3	8.458	.8246	605	46.8	63.6	1.4231
-43.4	46.0	8.797	.8015	585	46.34	63.5	1.4864
-60.6	45.6	9.261	.7819	562	46.6	63.0	1.5481
-79.8	45.3	9.806	.7582	543	45.8	62.7	1.6118
-100.3	45.0	10.285	.7396	525	46.0	62.3	1.6578
-110	45.1	10.655	.7308	504	45.6	61.8	1.6806

Table 1: Measured resistance value of different resistors

Figure 22. Percentage change in resistance from 24C to -110C

Polycide, Poly RN and Poly RP type resistors are quite stable, while SN, N+, P+ and PL type resistors change more significantly at lower temperatures. A changing resistance can change circuit voltages and currents at lower temperatures. Hence while designing circuitry for the mars transceiver stable resistors should be chosen or else a combination to form a stable resistor should be used. Alternatively a positive temperature coefficient of resistor such as P+ or N+ type could be used in an amplifier to

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stabilize gain (as transconductance will increase at low temperatures).Table 2 lists the measured temperature coefficient of resistance (1/deg Celsius) at reference temperature of 24˚C for various resistors.

Resistor	Temperature Coefficient of Resistor
Polycide	0.000392
N+	0.001445
P+	0.001348
Poly RN	0.000373
Poly RP	0.000279
SN	-0.00259

Table 2: Temperature Coefficients of resistance for various resistors

D. *Capacitors*

MOSFET capacitors are used in receiver and transmitter circuitry as high value bypass and coupling components. Like the resistors, capacitors tested at low temperatures refer to the capacitors on the Peregrine Semiconductor wafer. There are two types of capacitors on this wafer – RN and RP. The size of both capacitors is same 100/100. These types of capacitors are formed by connecting the source and the drain, of a MOSFET, as one terminal and then using the gate as other terminal as shown in Figure-23. A positive voltage needs to be applied to the gate for the case of RN capacitor so as to turn it on and vice versa for the PFET.
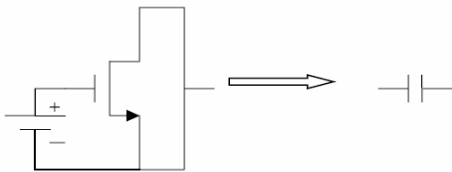

Figure-23 RN Capacitor

A test set for an RN capacitor was done using an HP 8753 network analyzer and reading the S11 values on a smith chart. The span was set from 100 MHz and 400 MHz and data was recorded at 100MHz and 400 MHz. S11 data consists of real part (R) and imaginary part (Xc) of the impedance Z. The capacitor value in these data sets correspond to the capacitance calculated by the formula ($C = 1/2\pi f \ Xc$) Where Xc is the magnitude of the impedance Z. A positive voltage of 3V with respect to drain and source was applied to the gate terminal using a bias tee. Network analyzer was calibrated using a calibration board having a surface mount resistor of 50Ω for the load condition. The table below presents data obtained from the cryogenic testing of the RN capacitor at 100 MHz and 400 MHz.

Temperature (˚C)	Real (100Mhz)	Real (400 Mhz)	Imaginary (100 Mhz)	Imaginary (400 Mhz)	C Value (pf) (100MHz)	C Value (pf) (400MHz)
26	177.5	93.2	-169.3	-80.3	9.3	4.9
0	169.5	88.5	-162.05	-76.5	9.8	5.18
-20	165.5	86.5	-155.47	-73.9	10.2	5.3
-40	160.5	87.1	-152.7	-72.0	10.4	5.5
-60	159.3	83.3	-147.5	-70.7	10.7	5.6
-80	158	85.4	-135.2	-64.5	11.6	6.1
-100	141.3	76.2	-132.1	-62.3	12.0	6.3
-120	141.4	75.8	-131.0	-61.1	12.2	6.5

Table 3 Impedance of RN Capacitor

The capacitance increases with decrease in temperature. As seen from the data from Table-3 the capacitance values are different at 100 MHz and 400 MHz, while it is supposed to remain constant. An investigation in to this problem concluded that a MOS capacitor at high frequencies is not a capacitor since its channel resistance starts affecting its measured reactance value and hence a capacitor at high frequencies is capacitor in series with a resistor. The decrease in capacitance is because of the decrease in the channel resistance at these frequencies. The capacitor model at high frequencies looks more like the one shown below.
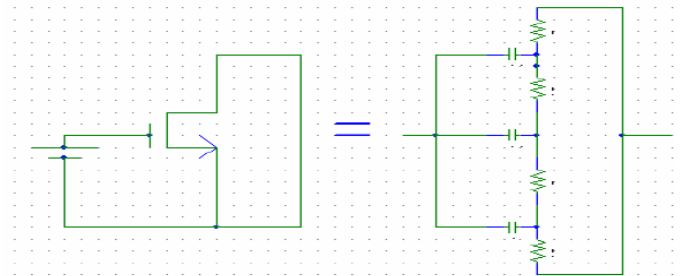

Figure 24. RN capacitor at high frequencies

The test results for RP capacitors are listed in Table-4. While the changes in capacitance appear large, they can be significantly reduced using different aspect ratio devices from the 100/100 MOSFETs available on the test wafer.

Temperature	Real (100Mhz)	Real (400 Mhz)	Imaginary (100 Mhz)	Imaginary (400 Mhz)	C Value (pf) (100MHz)	C Value (pf) (400MHz)
26	245.18	124.82	-231.09	-111.76	6.88	3.55
0	234.00	120.30	-219.09	-106.23	7.25	3.74
-20	226.21	116.90	-209.73	-101.61	7.58	3.91
-40	215.92	112.63	-200.09	-96.88	7.95	4.10
-60	206.52	108.37	-190.13	-91.87	8.36	4.33
-80	197.59	104.56	-181.58	-88.02	8.75	4.52
-100	188.34	100.70	-171.94	-83.43	9.24	4.77
-120	182.95	97.05	-166.09	-80.29	9.65	4.95

Table -4 Impedance of RP capacitor

E. *MOSFETs*

The wafer from Peregrine-Semiconductor has various flavors of MOSFETs (RN, RP, PL, NL, IN, IP etc) on its test structures. These MOSFETs were tested by using an automated curve tracer LabVIEW program. Like resistors and capacitors, MOSFETs are a basic element of any circuit design and thus also needed to be performance characterized at low temperatures. The threshold voltage and the drain current variation are the major characteristics used in the

circuit design. The following V_{gs} Vs I_d curves were generated for varying V_{ds} values at different temperatures. As expected the threshold voltage and the drain current increases with decrease in temperature.
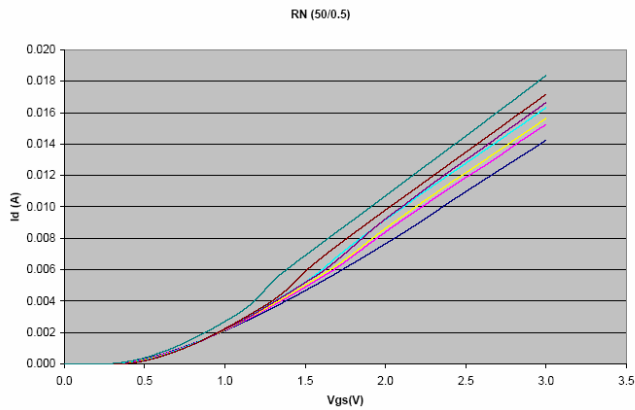

Figure 25. V_{gs} Vs I_d Curves for RN (50/0.5) MOSFET at V_{ds} = 3V

Measurements were also taken at V_{ds} = 2.5V, 2V, 1.5V, 1V, 0.5V. Figure 26 shows the curves between V_{ds} and I_d by changing different values of V_{gs}.
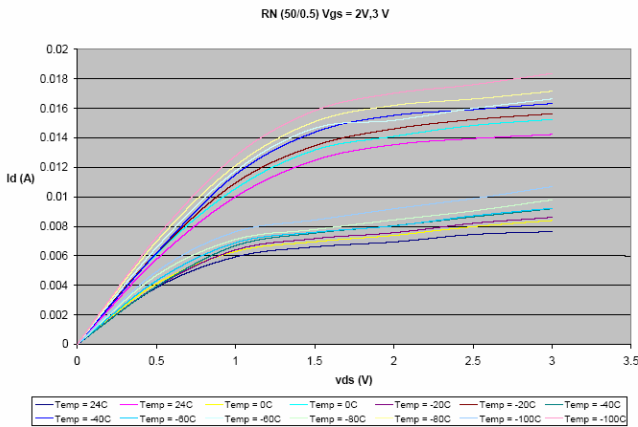

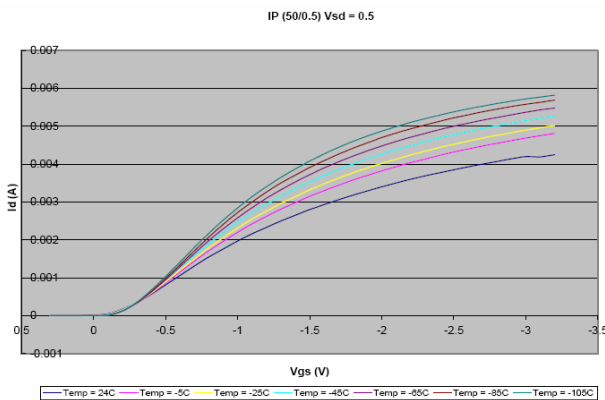Figure 26. Vds Vs Id Curves for RN (50/0.5) MOSFET at Vgs = 2.0, 3.0 V

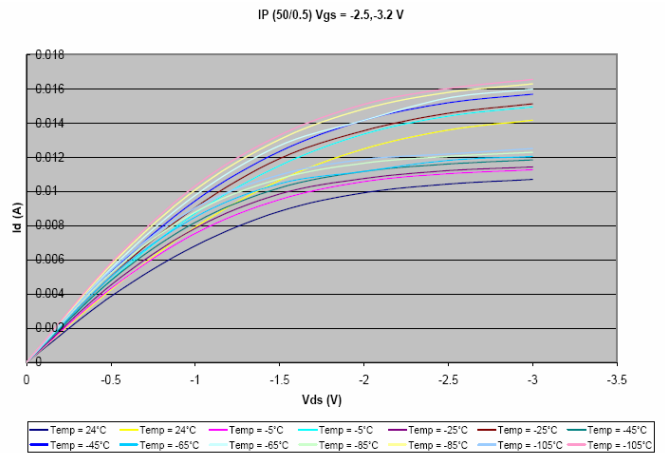Figure 27. 10. V_{gs} Vs I_d Curves for IP (50/0.5) MOSFET at V_{sd} = 0.5 V

Figure 28. Vds Vs Id Curves for IP (50/0.5) MOSFET at Vgs = -2.5,3.2 V

V. SUMMARY AND CONCLUSIONS

A reliable cryogenic test bench has been developed during the course of this research. The data obtained from the testing of various COTS electronic components, both off-chip, and on-chip, have shown that it is feasible to operate these components at Martian temperatures after some special design consideration. Some conclusions for the use of COTS electronic components at extreme low temperatures include.

1. TCXOs and ceramic filters both shift downwards in frequency and thus favor a high-side injection scheme in a super-heterodyne receiver.
2. The total shift in center frequency of the IF ceramic filter is less than half the bandwidth and thus we can use lower bandwidth receiver architecture.
3. To achieve a stable resistor at lower temperature it is possible to use a resistor having a positive coefficient of resistance with a resistor having negative coefficient of resistance so that the overall effect results in a stable resistor.
4. The mobility and increase in threshold of the NFETs and PFETs can be offset by the use of appropriate resistor coefficients to stabilize circuit biasing and gain.

The test data obtained from various COTS electronic components can be used for designing digital and analog circuits at lower temperatures and thus will prove resourceful to the designers at NASA or elsewhere.
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BIOGRAPHY
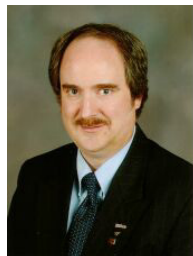
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