



# A Low-Power, Radiation-tolerant, RFIC Micro-Transceiver

**William Kuhn, Jeongmin Jeon, and Kai Wong**

Kansas State University

Department of Electrical and Computer Engineering

**13th NASA Symposium on VLSI Design**

**Post Falls, Idaho**

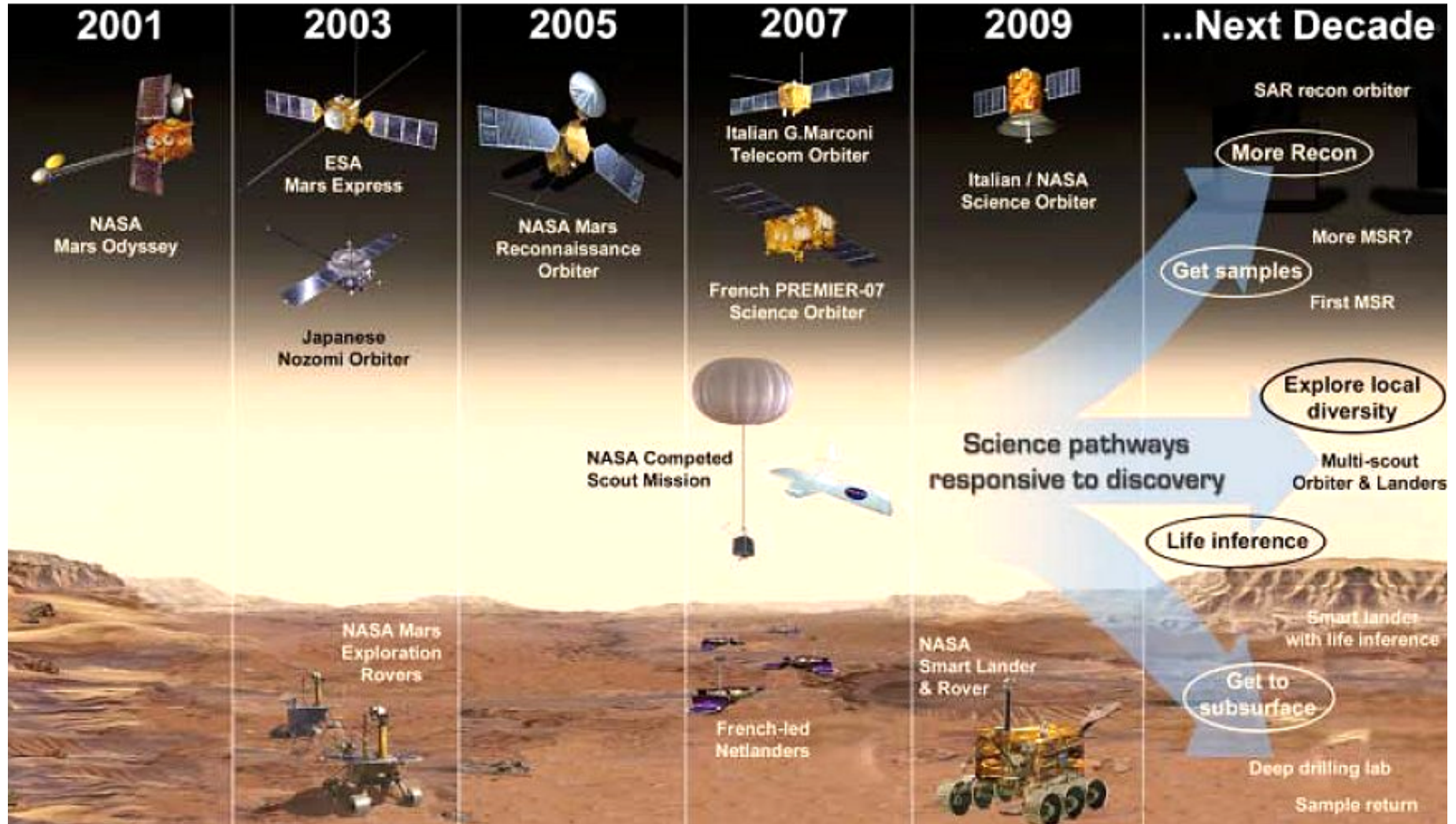
**June 5 & 6, 2007**



# Mars Exploration Timeline

MEP Advanced Technologies NRA 03-OSS-01

Telecommunications and Tracking



Multimedia courtesy of Caltech's Jet Propulsion Lab and NASA



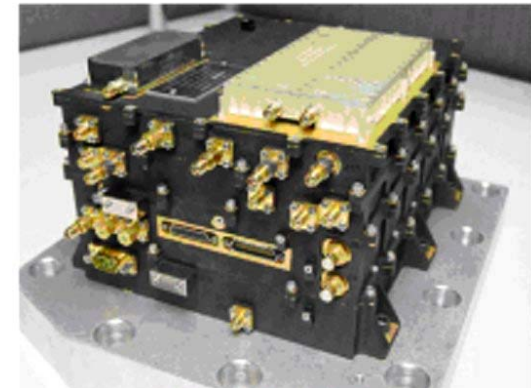
# Problem Statement



**Develop a highly-miniaturized, extremely low-mass, low-power UHF Micro-transceiver module for *aerobots, microrovers, penetrators, and small networked landers.***

## Key Challenges, Benefits, and Tradeoffs

- Existing transceivers (e.g. C/TT-505) measure 2000 cm<sup>3</sup>, weigh 2 kg, and draw up to 60 Watts on transmit and 6 Watts on receive.
- Target volume and mass of microtransceiver is approximately 5 cm<sup>3</sup> and 5 grams (50 grams) for PC board (metal-housed) form-factor implementations.
- Target power consumption is 50 mW on receive (< 1 mW using sleep mode), and 100 mW / 300 mW / 3 W on transmit for 10 mW / 100 mW / 1 W output.
- Mission tradeoffs include reduced data-volume return at lower transmit powers, half duplex operation, and limited packet handling/formatting, in exchange for one to three orders of magnitude reduction in mass, volume, and power.



**Electra UHF Transceiver**  
(p/o MRO relay to earth)



**Electra-Interoperable UHF Microtransceiver**

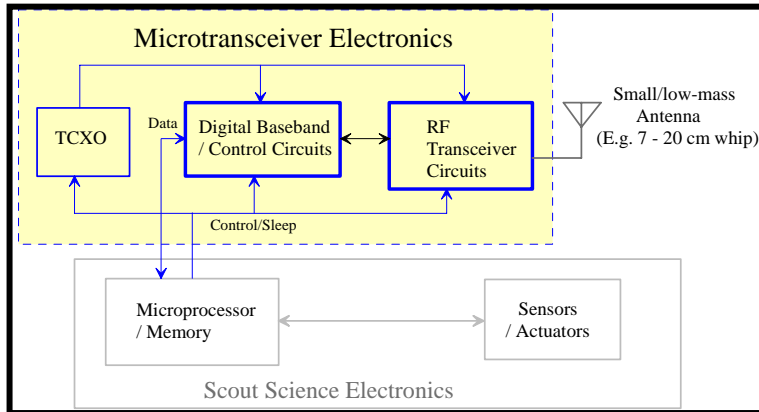




# Micro-transceiver Development

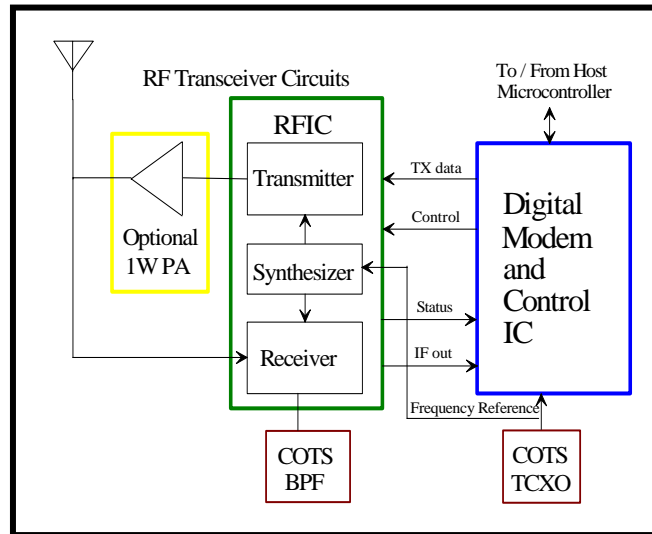


## Top Level Block Diagrams



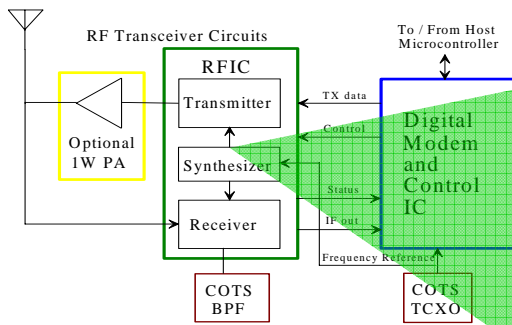
## Size/Mass/Power Reduction Techniques

- Design employs a two/three chip solution
- Off-chip components limited to Commercial Off-The-Shelf (COTS) IF filter and TCXO
- RFICs employ full-custom design in Silicon-on-Sapphire process for good RF performance and radiation hardening
- Analog/RF circuits and COTS parts characterized to -100 C to enable operation outside warm-box in some applications
- Digital modem/control circuits designed by JPL will employ low-complexity design techniques and implement subset of Prox-1 space-link protocol
- Higher level protocols will be assumed by host system microcontroller



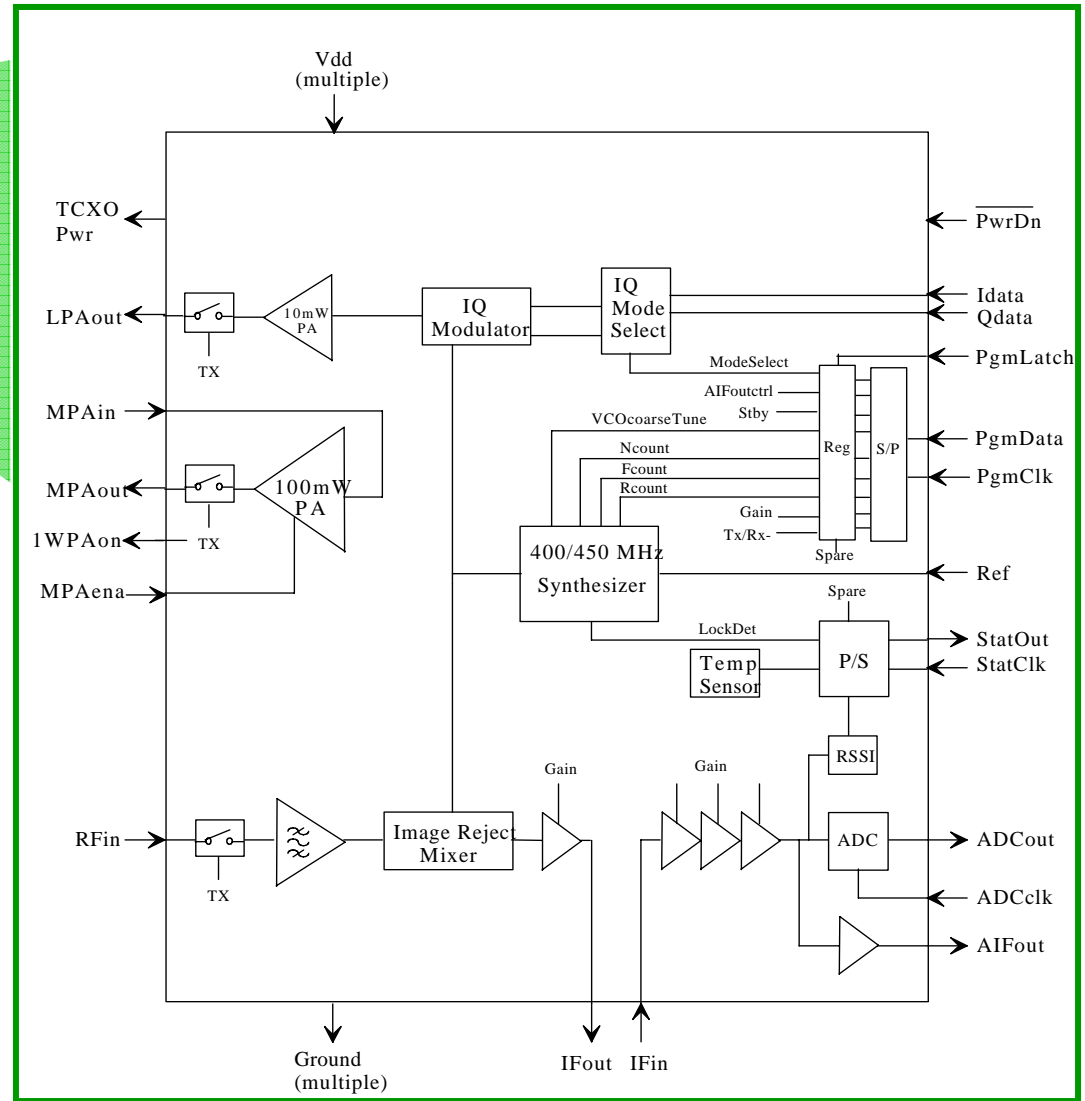


# RFIC Development Technical Approach



## RFIC Design Techniques

- Proven/robust architectures employed (superhet receiver and direct modulation transmitter)
- New techniques developed for TR switching and integrated watt-level power amp
- Transmitter employs large size, high-Q inductors to achieve good efficiency
- Receive trades off image rejection, IP3, and compression performance for low power
- Half-duplex operation allows transmitter and receiver on same die
- IF sampling allows companion digital modem IC to provide high-quality detection with multiple modulation types





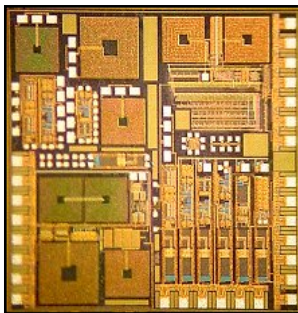


# Iterative Prototyping – the key to success

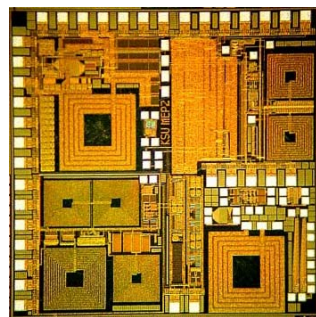


## Scheduled Fabrication Runs

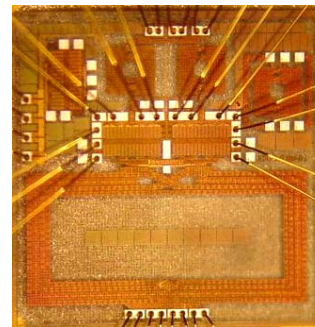
1. RFIC receiver blocks and temp-stable bias circuits	Mar 05	4. Full-transceiver RFIC (100 mW die)	Sep 06
2. 1 <sup>st</sup> RFIC receiver prototype + 100mW PA prototype (+ LNA 2 <sup>nd</sup> spin + SD PLL prototype)	Sep 05	5. Digital receiver and control circuits	Mar 07
3. 1W PA prototype	Mar 06	6. Re-spin as needed	Variable



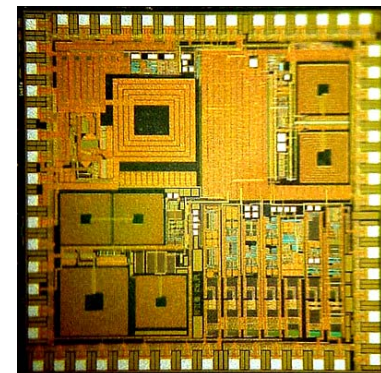
**Fab 1 Receiver**  
March 2005



**Fab 2 Transmitter**  
Sept 2005



**Fab 3 1-Watt PA**  
March 2006



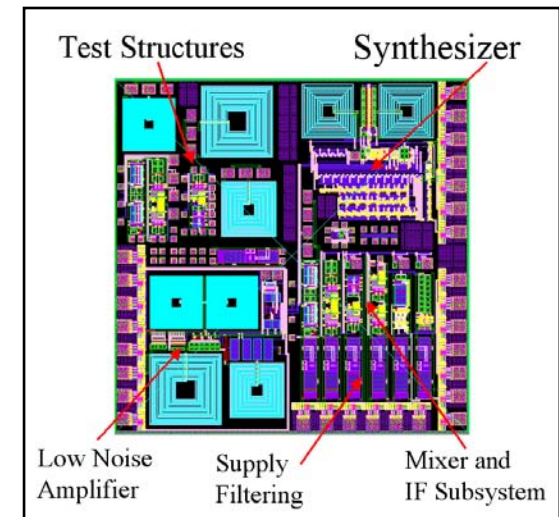
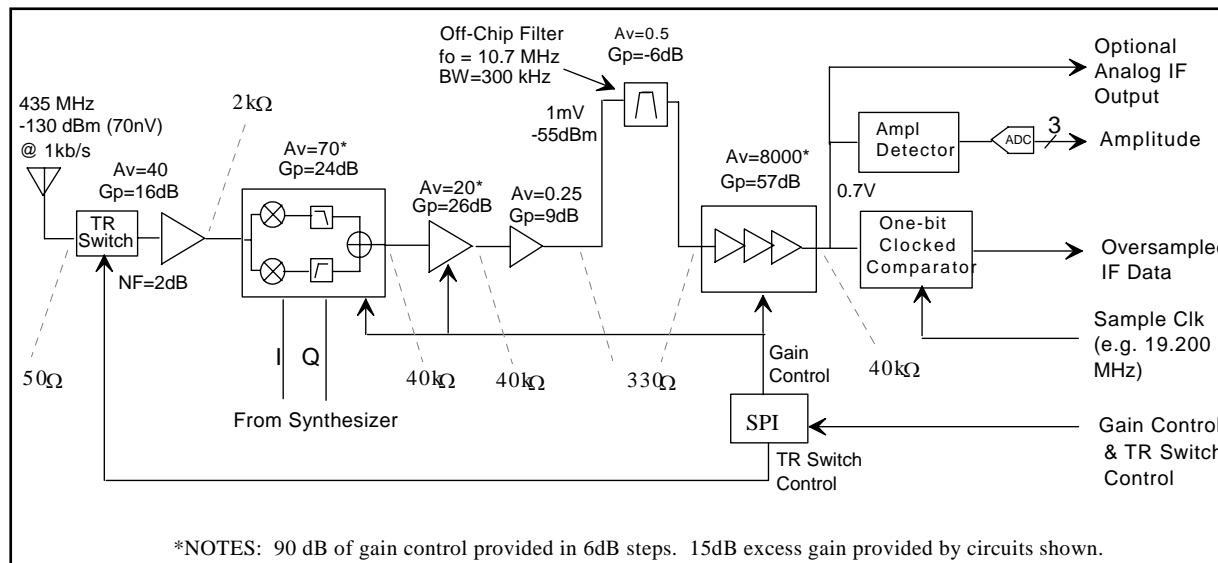
**Fab 4 Transceiver**  
Sept 2006



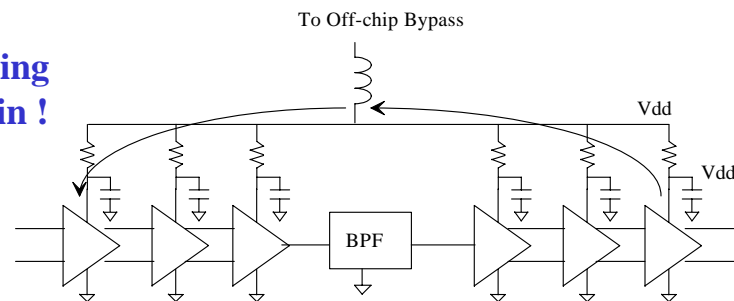
# RF Integrated Circuit Development



## Fab 1 Receiver Prototype Circuit Design (March 2005)



Careful on-chip supply filtering provided in IF amplifier chain !



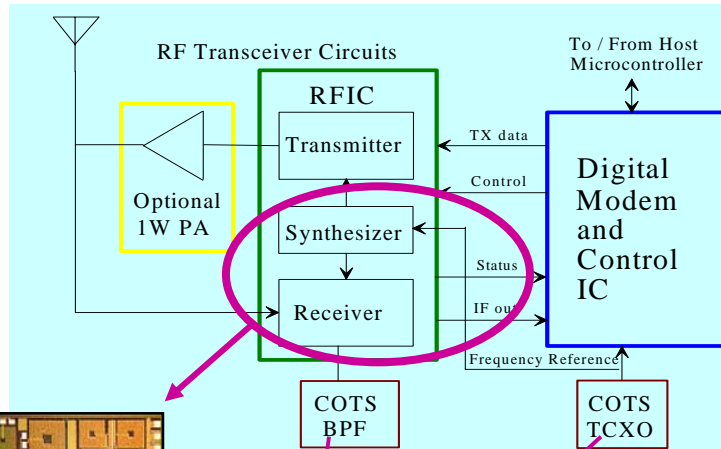
Fab-1 Die Layout



# RF Integrated Circuit Development

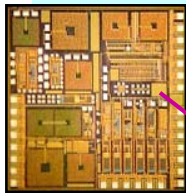


## Fab-1 Receiver Prototype Testing (Summer/Fall 2005)

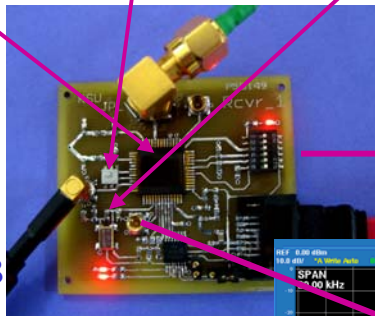


- Successfully tested from RF-in to sampled IF-out
- Low temperature testing showed nominal behavior to  $-100^{\circ}\text{C}$  with low parametric drift
- Identified areas needing improvement in subsequent fabs to fully meet performance goals:

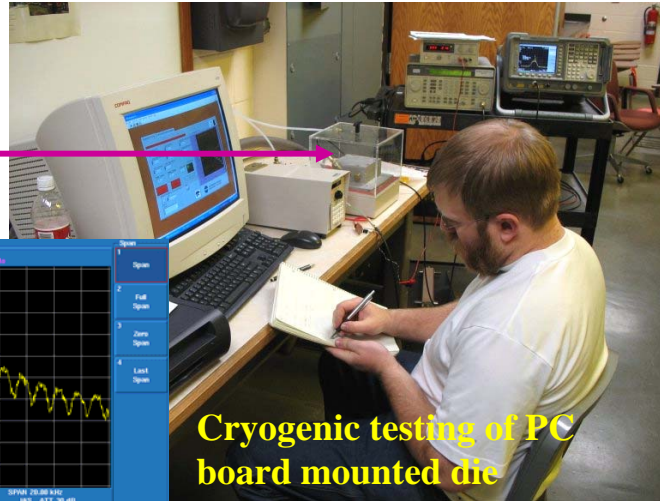
1. Improve LNA gain to achieve system NF spec
2. Provide finer tuning steps and reduce spurs



Fab1 die

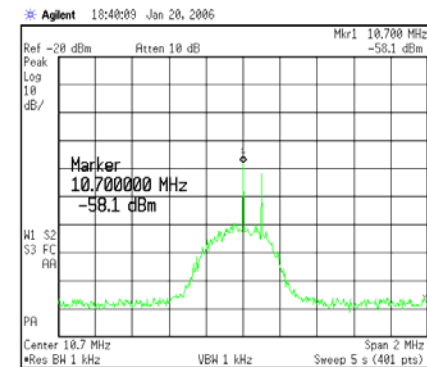
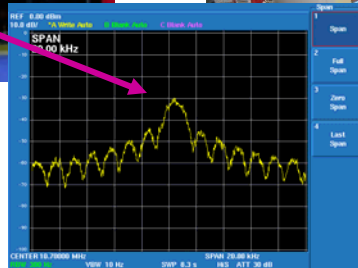


Packaged die on PCB



Cryogenic testing of PCB board mounted die

Spectrum of 1-bit ADC output (1.5 kbps QPSK)



IF filter output from  $+25^{\circ}\text{C}$  to  $-100^{\circ}\text{C}$  with  $-100\text{ dBm}$  unmodulated carrier. (reference harmonic spur visible to right)

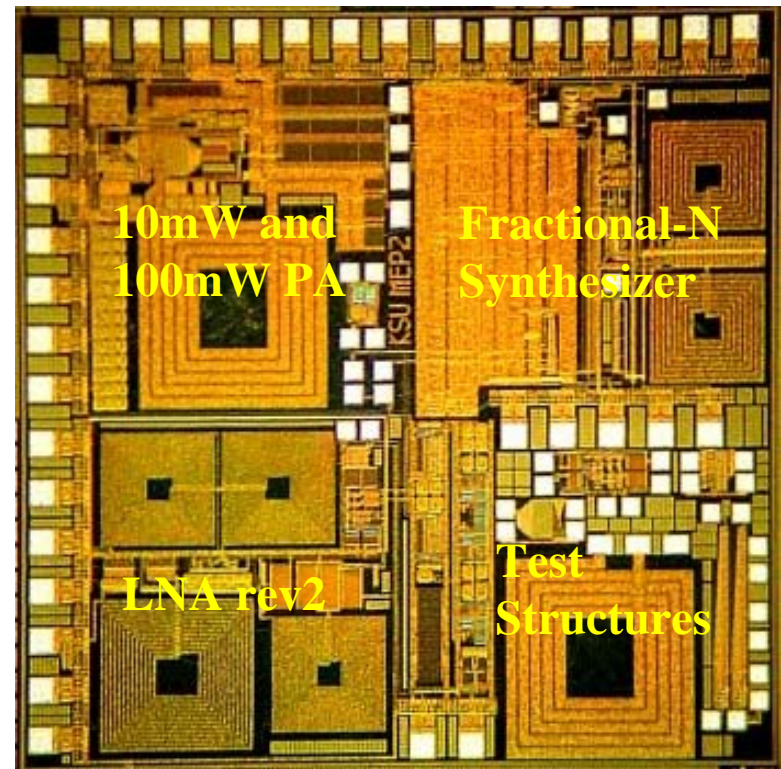
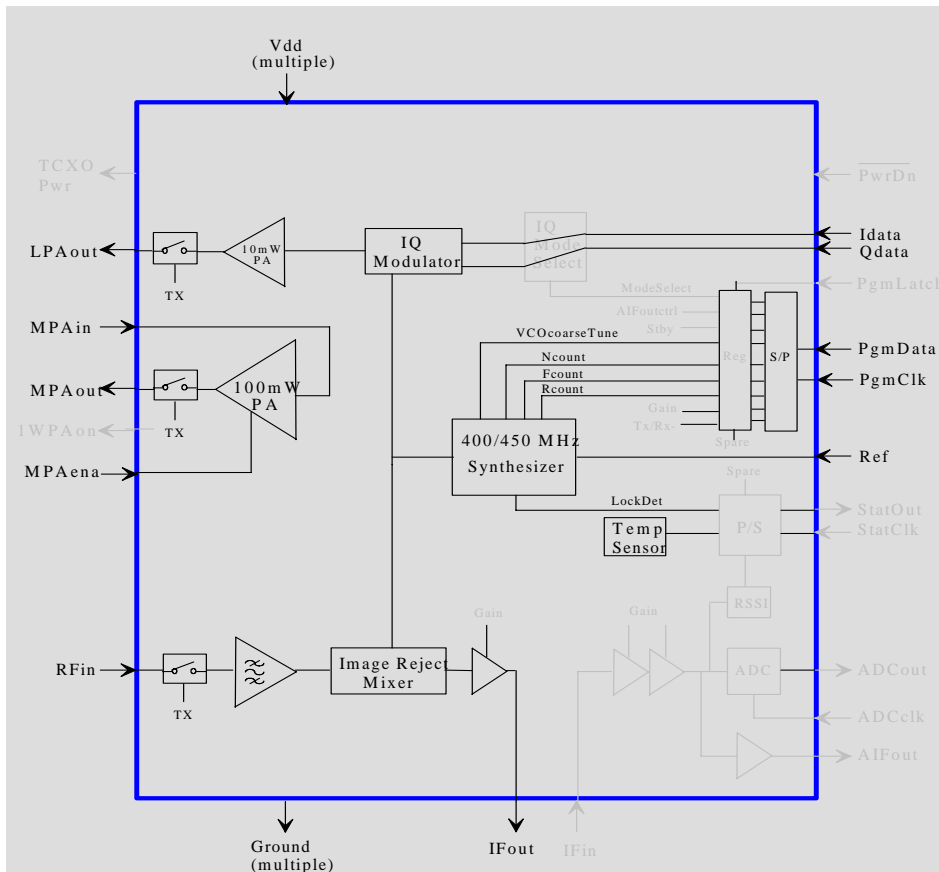




# RF Integrated Circuit Development



## Fab 2 Transmitter RFIC Circuit Tapeout (March 2006)

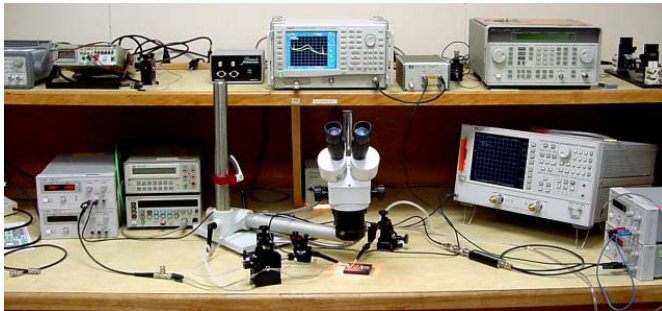


Fab-2 Die Photo

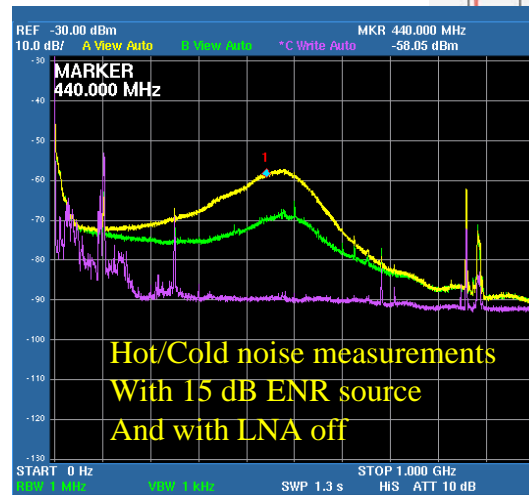
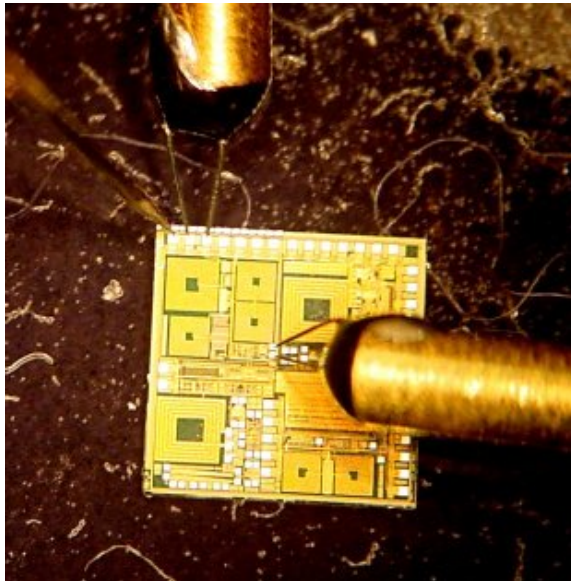
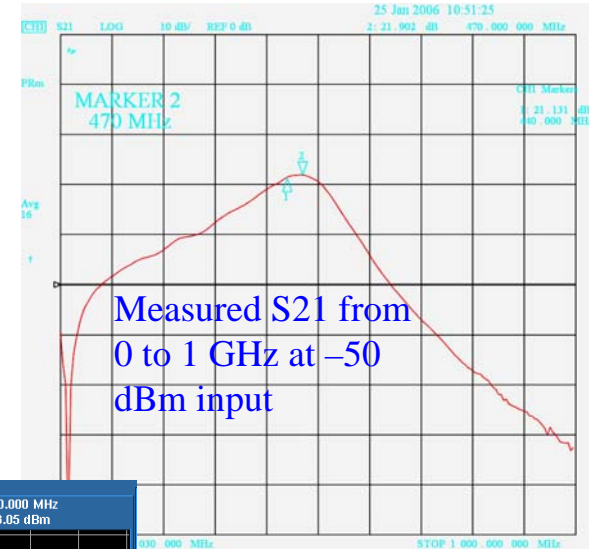


# Fab-2 Chip Testing

## LNA Re-spin Successful ☺



- Gain > 22 dB
- S11 < -10 dB
- I<sub>dc</sub> = 3 mA (est.)
- 1dBc = -40 dBm



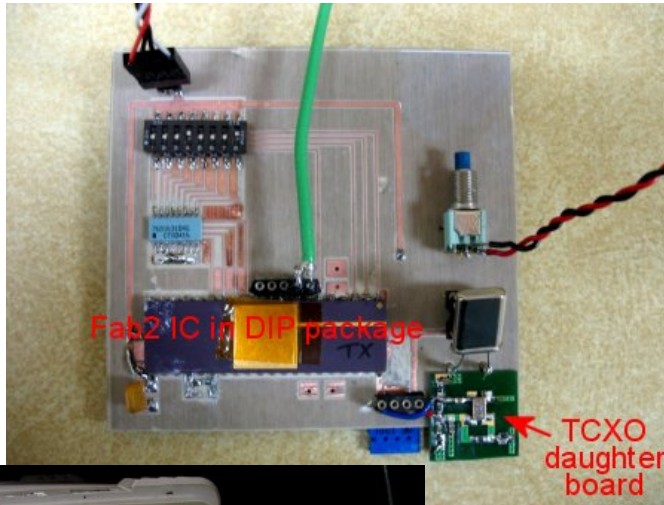
- NF = 3.4 dB at 25C
- Calculated NF < 2.6 dB at -60C



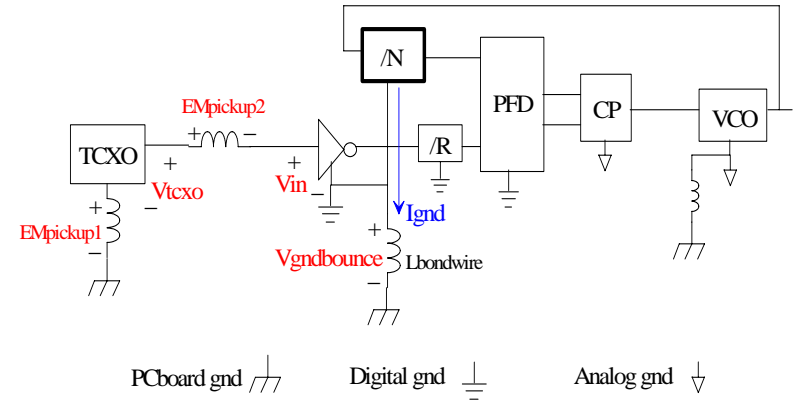
# Fab-2 Chip Testing Problems



## Phase-lock problems encountered with early PCBs ☹

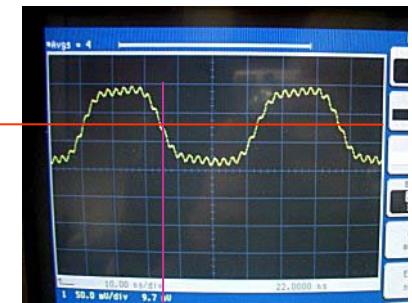


Unlocked spectrum



$$V_{in} = V_{tctxo} - V_{gndbounce} + (EMpickup1 - EMpickup2)$$

Vin threshold



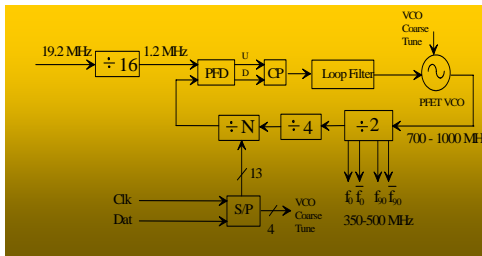
Phase-variation from added  
400 MHz signal  
⇒ Modified feedback in loop  
⇒ Loss-of-lock



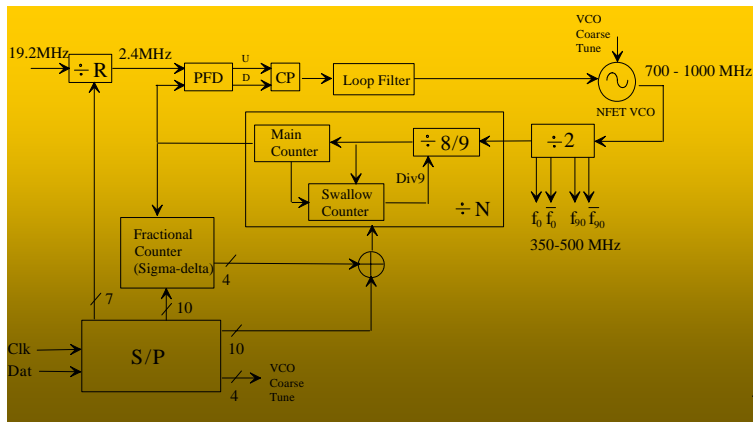


# Fab-2 Chip Testing

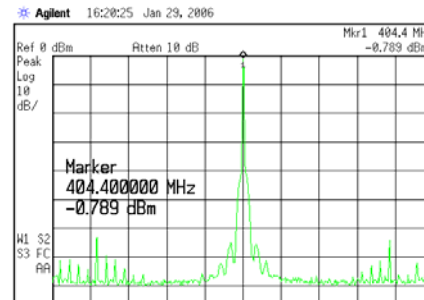
## Fractional-N Synthesizer Operational after PCB mods (Phase Noise, Spurs, and Power Consumption Acceptable)



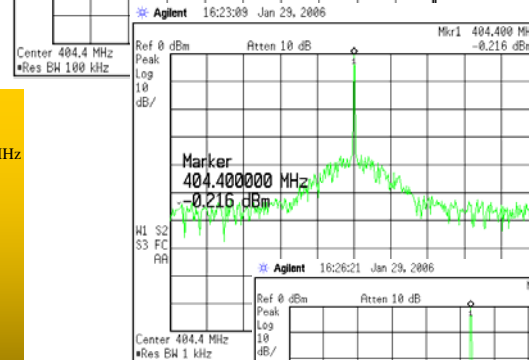
Fab-1 Integer-N Architecture  
Tuning step size = 4.8 MHz



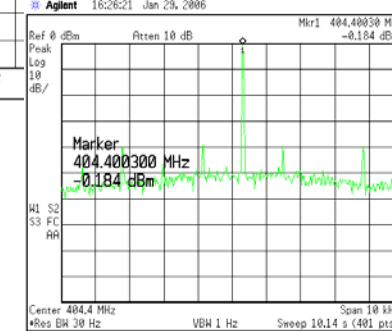
Fab-2 Fractional-N Architecture  
Tuning step size = 2.34 kHz



100 MHz Span  
100 kHz resolution



1 MHz Span  
1 kHz resolution



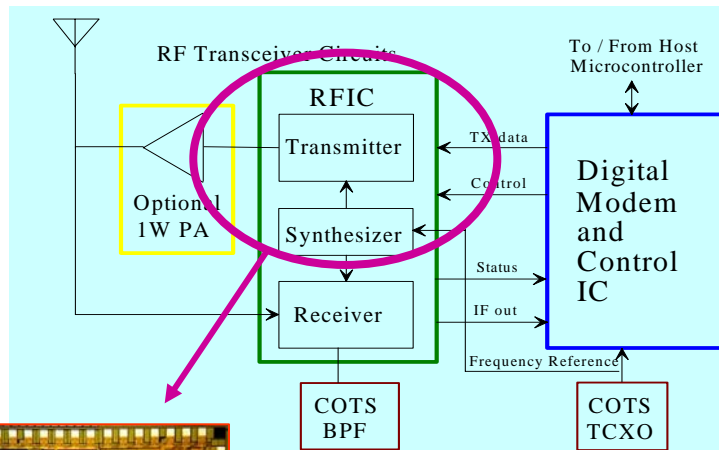
10 kHz Span  
30 Hz resolution





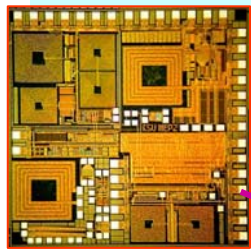
# Fab-2 Chip Testing

## Full Transmitter Spectrum and Constellation Tests



- All circuits operational and tested to -100 C
- Identified areas needing improvement in subsequent fabs to fully meet performance goals:

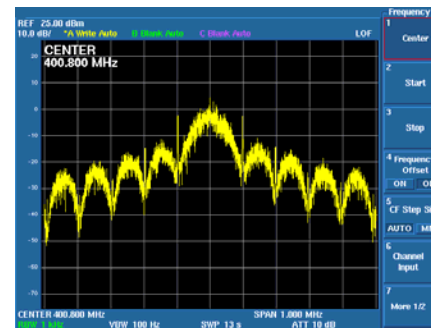
1. *Provide dedicated vdd/gnd pins to TCXO to address PLL locking problems*
2. *Increase PFD/CP current to allow wider loop bandwidth and reduce phase jitter and EVM*
3. *Provide dedicated ground on loop filter and more Vdd/Gnd bonds on PA to address constellation EVM problems*



Fab2 die



Packaged die on revised PCB



BPSK spectrum



Transmitter signal constellations (1kbps BPSK)



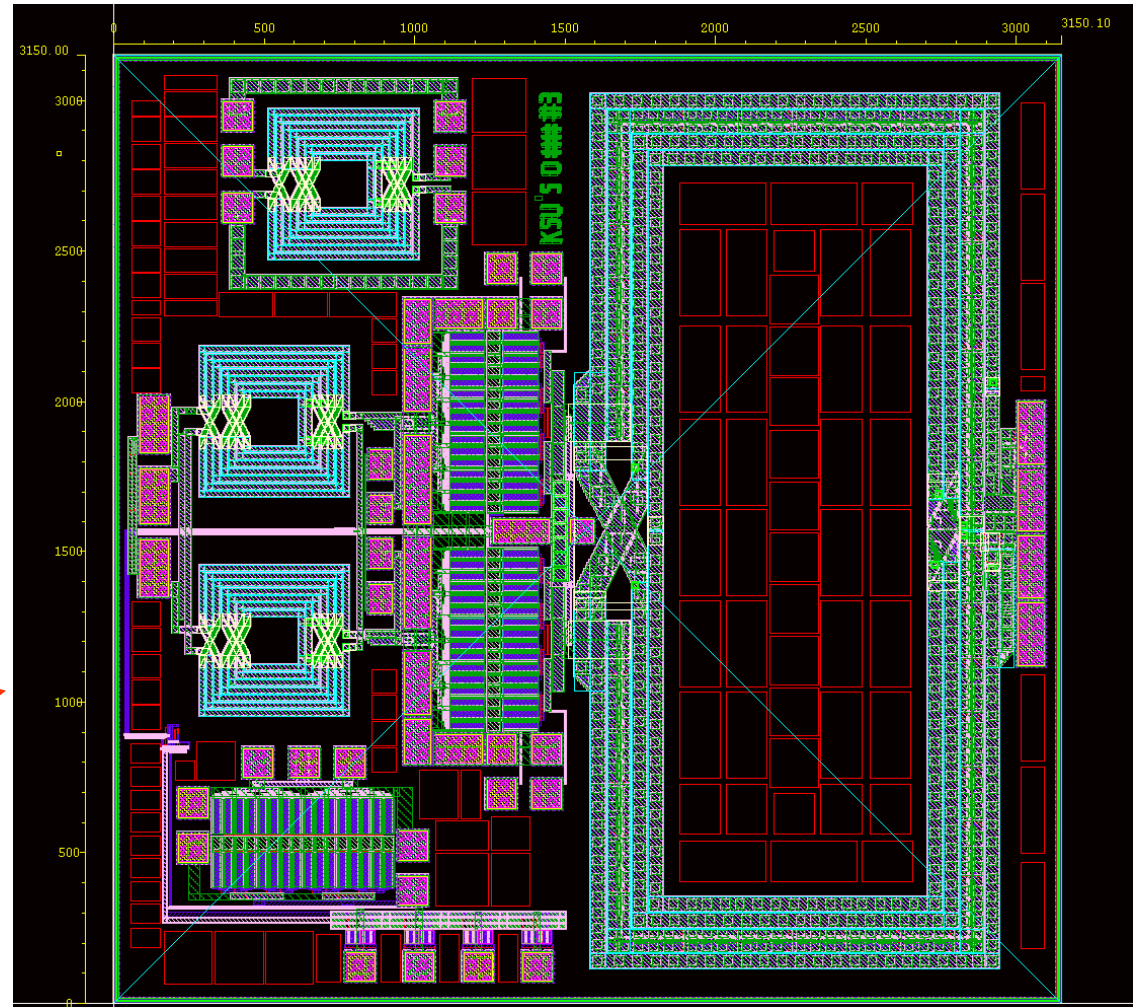
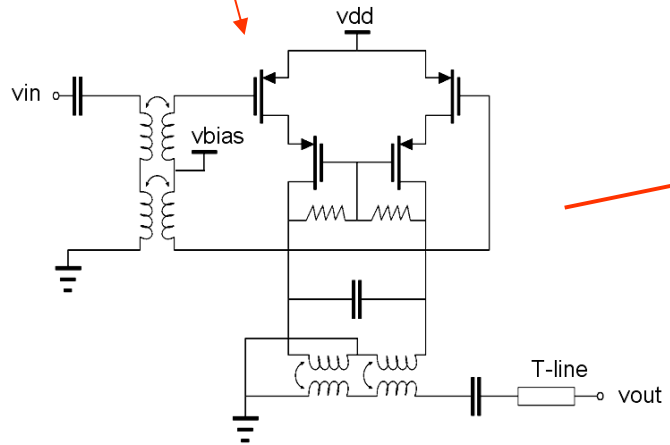
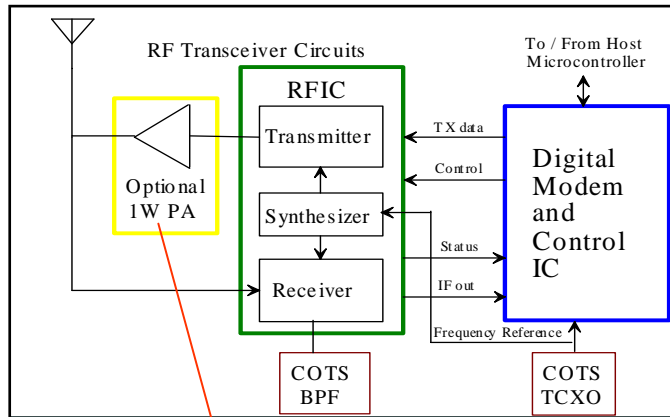
# RF Integrated Circuit Development



MEP Advanced Technologies NRA 03-OSS-01

Telecommunications and Tracking

## Fab-3: 1-Watt Transmitter Submitted in March 06



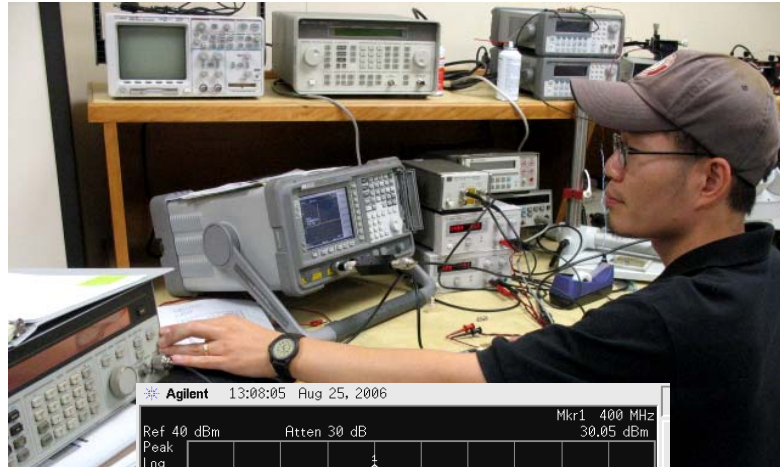
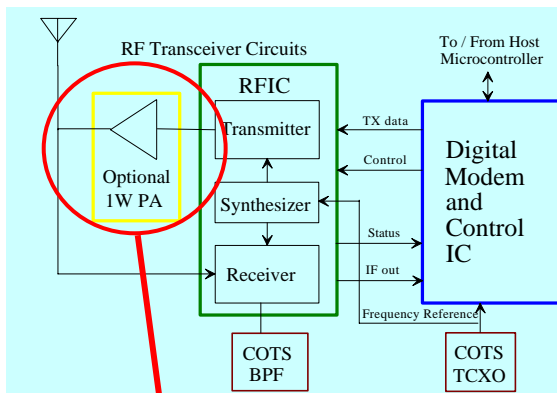


# Fab-2 Chip Testing



## Fab-3: 1-Watt Power Amplifier Successfully Tested

Microtransceiver Chipset Block Diagram



Measurement of PA output on spectrum analyzer.

- 20 dB attenuator protects instrument
- Offset of 20 dB added to display
- Accuracy approx +/- 0.5dB
- Meets spec, although some variation between die
- Tested to 4V for safety

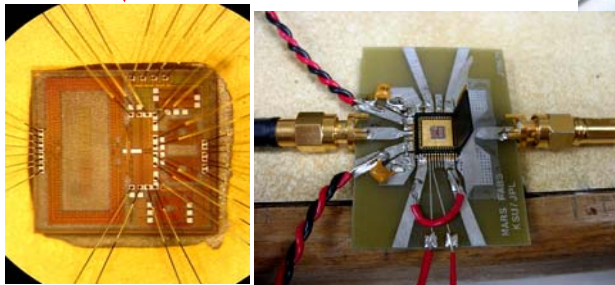
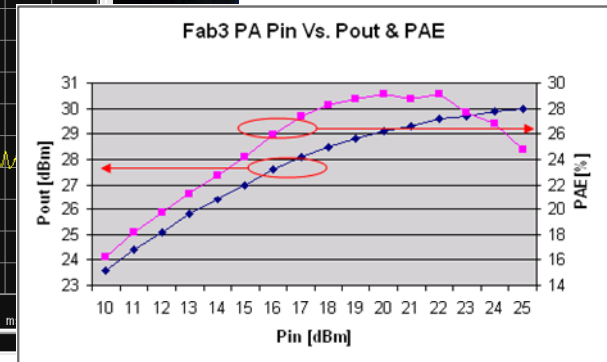
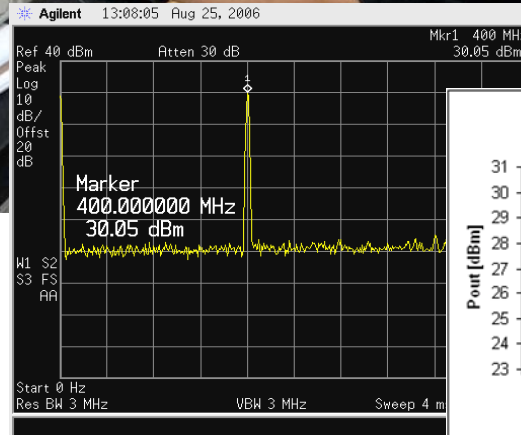


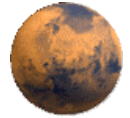
Photo of die mounted in package and package on PCB



Completes initial development of all major Microtransceiver RFIC prototype circuits.



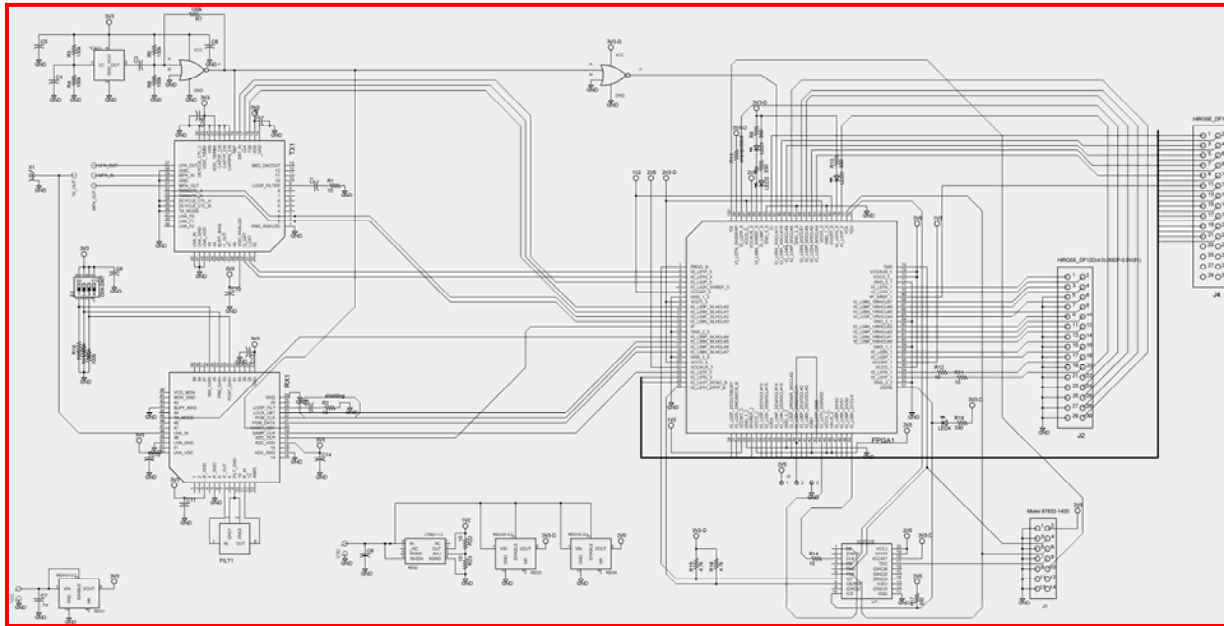
# System-Level Test Vehicle



MEP Advanced Technologies NRA 03-OSS-01

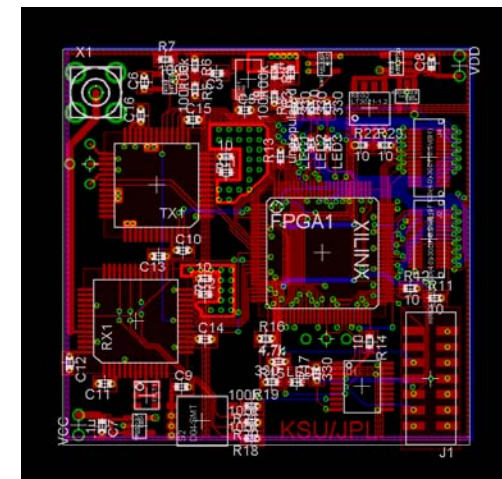
Telecommunications and Tracking

## K-State/JPL Transceiver Integration



4-Layer PCB Layout  
Approximate size = 5 x 5 cm

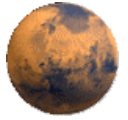
- PC board developed to allow hardware test of digital modem signal processing
- Will also allow early system-level hardware testing to investigate PCB noise issues
- Employs Fab1 Receiver and Fab2 Transmitter RFICs
- JPL will use Spartan 3E FPGA for digital circuit testing





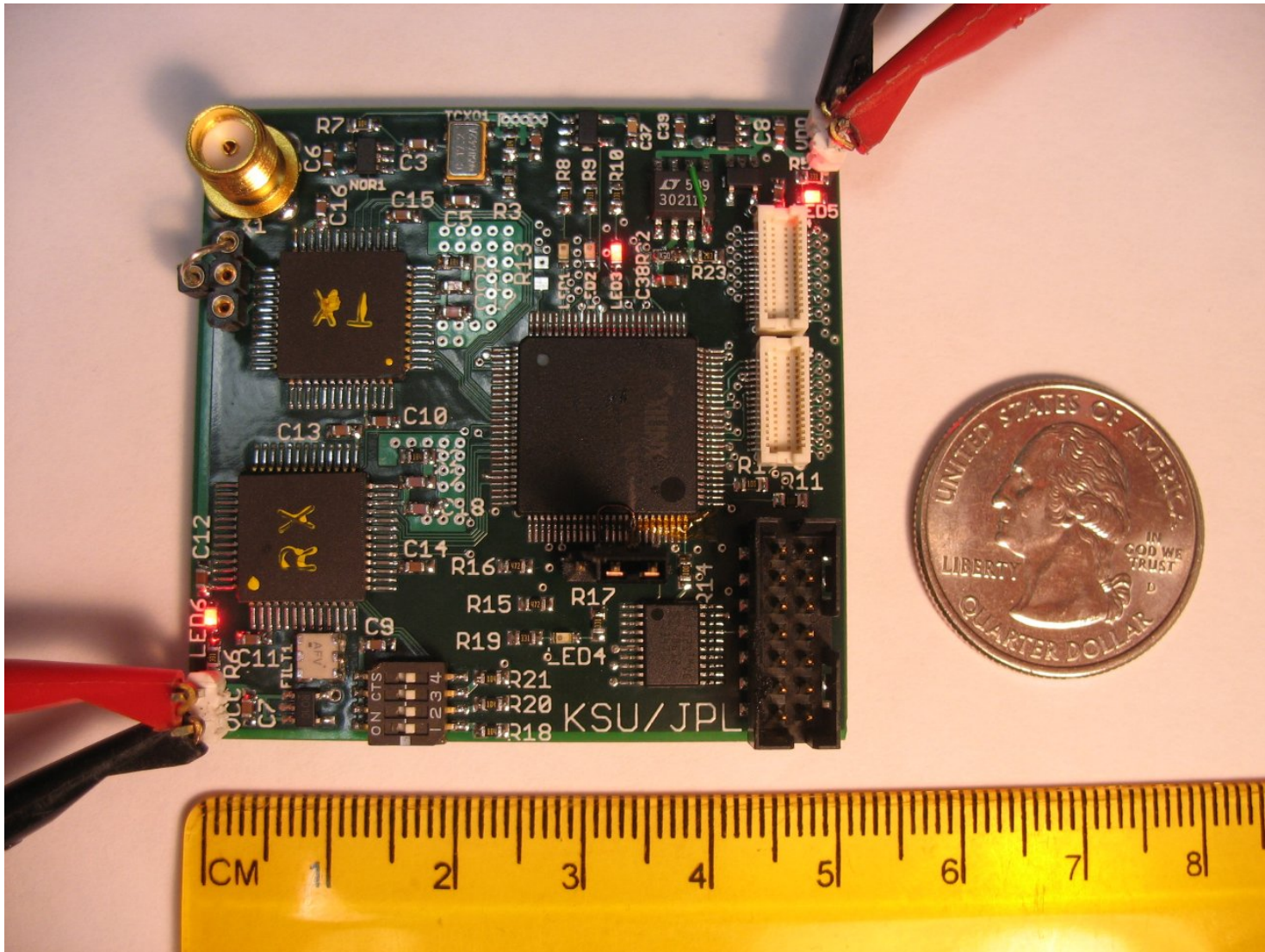


# System-Level Test Vehicle



MEP Advanced Technologies NRA 03-OSS-01

Telecommunications and Tracking

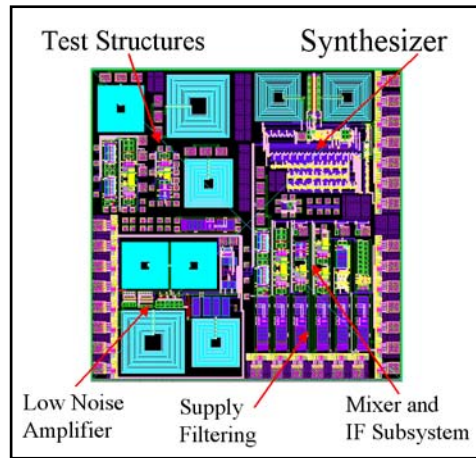




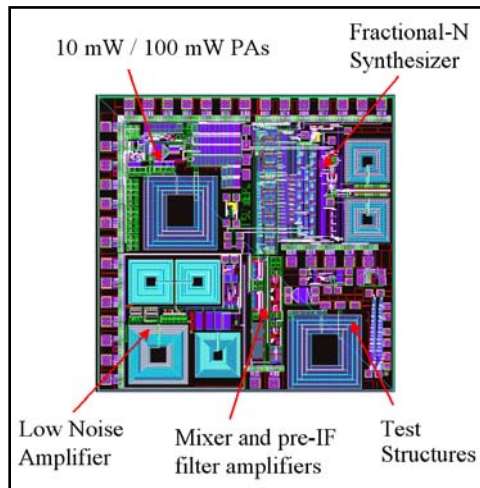
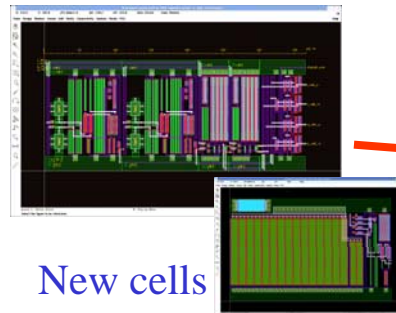
# RF Integrated Circuit Development



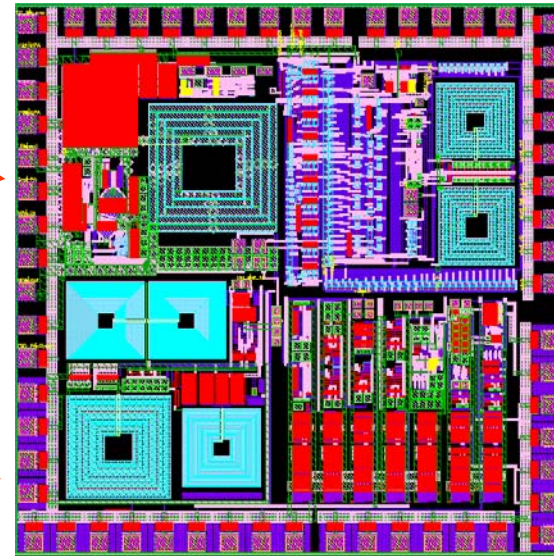
## Fab-4 Full Transceiver Chip (Fall 2006)



Fab1 die (Mar 05)



Fab2 die (Sept 05)



Fab4 die (Sept 06)

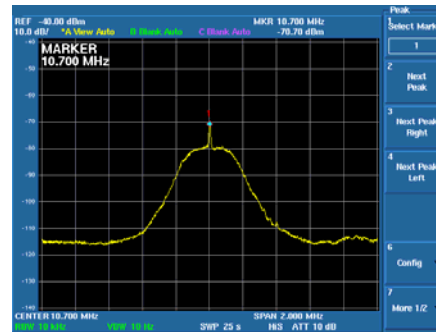
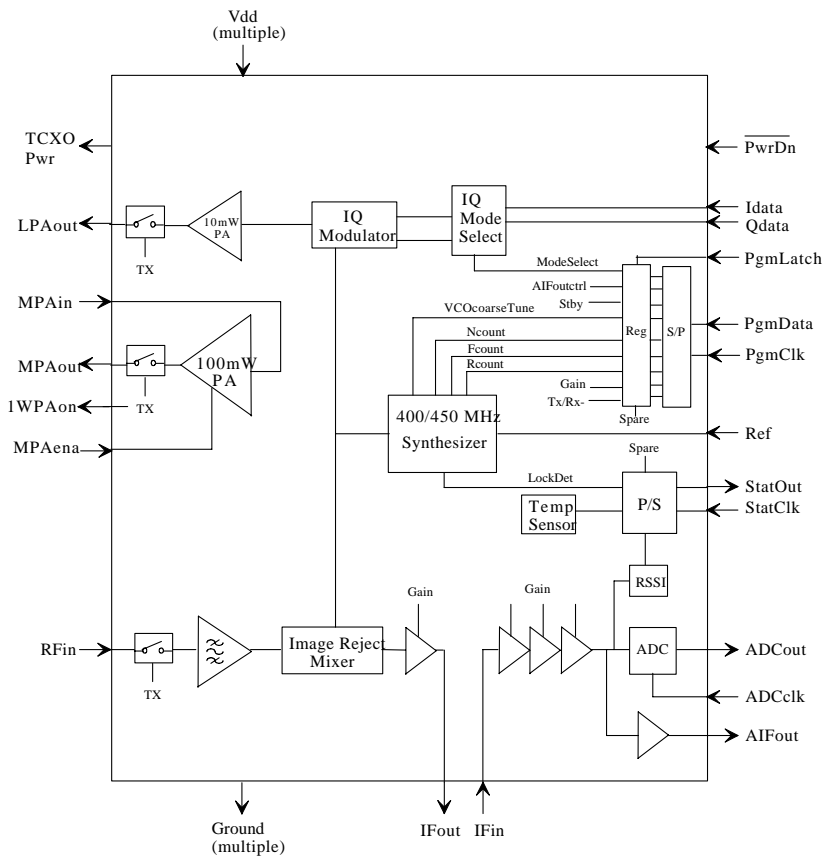
- Die size increased to 3.2 x 3.2 mm, 60 pins
- Corrected problems found during fab-1 and fab-2 testing, adding differential signaling, extra pwr/gnd pins, etc.
- Added analog IQ modulator inputs, analog IF output, temperature sensor, lock detector, standby current mode, and full digital control (programming and status registers).



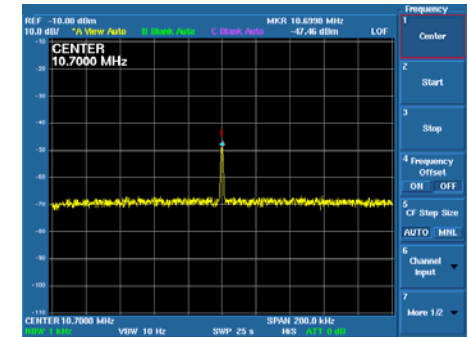
# Fab4 Initial Performance Assessments



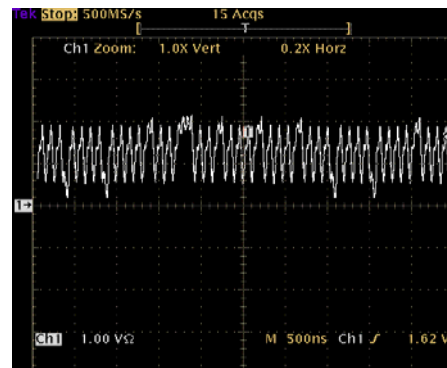
## Fab4 Test Results (2007)



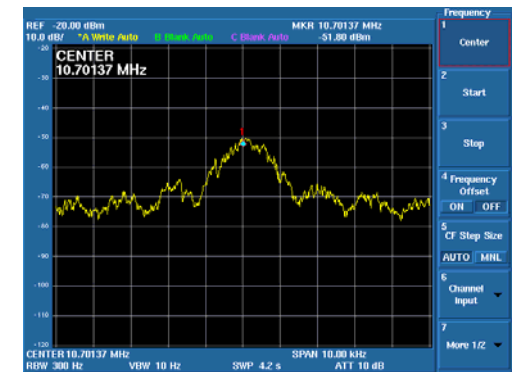
-120 dBm RF signal converted to 10.7 MHz IF at 10 kHz RBW, demonstrating full sensitivity.



-120 dBm RF signal converted to 10.7 MHz IF at 1 kHz RBW, validating 3 dB noise figure and no in-band spurs (this plot does not include switch losses)



1-bit ADC output datastream with 19.2 MHz sample rate. Single-ended output shown.



Spectrum analyzer view of 1-bit ADC output bitstream validating end-to-end receiver operation.





# Fab4 Test Results Summary



## Tested Items

- Serial to parallel programming registers
- Power-on resets
- TCXO clock output
- VCO coarse and fine tuning
- BPSK and RC-BPSK modulation (including new line receivers)
- 10 / 100 mW PA outputs
- TR switch on both TX and RX modes
- Receiver, through IF filter
- ADC output
- Analog IF output
- Synthesizer reference divider
- PFD/CP output
- Status register output
- Lock detect (design problem found)
- Nominal current consumption

\***Green** = working

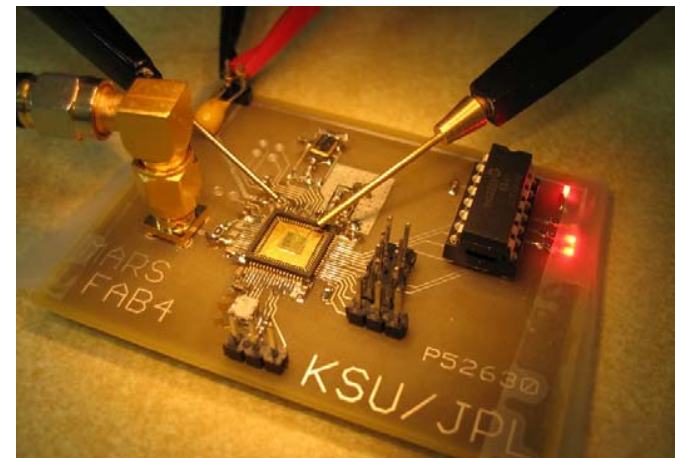
\***Red** = problem found  
(will be fixed in 2007 fab when additional refinements are also made)

## Items being debugged

- Some constellation issues in 100 mW mode

## Items not yet tested

- Analog modulation inputs
- Temperature sensor
- Power down switch circuits
- ESD tolerance on RF input
- Temperature tolerance







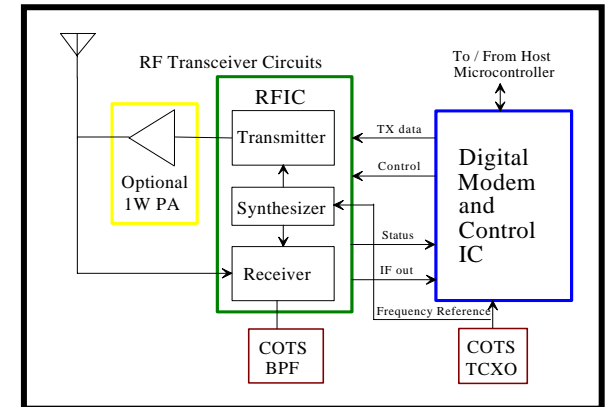
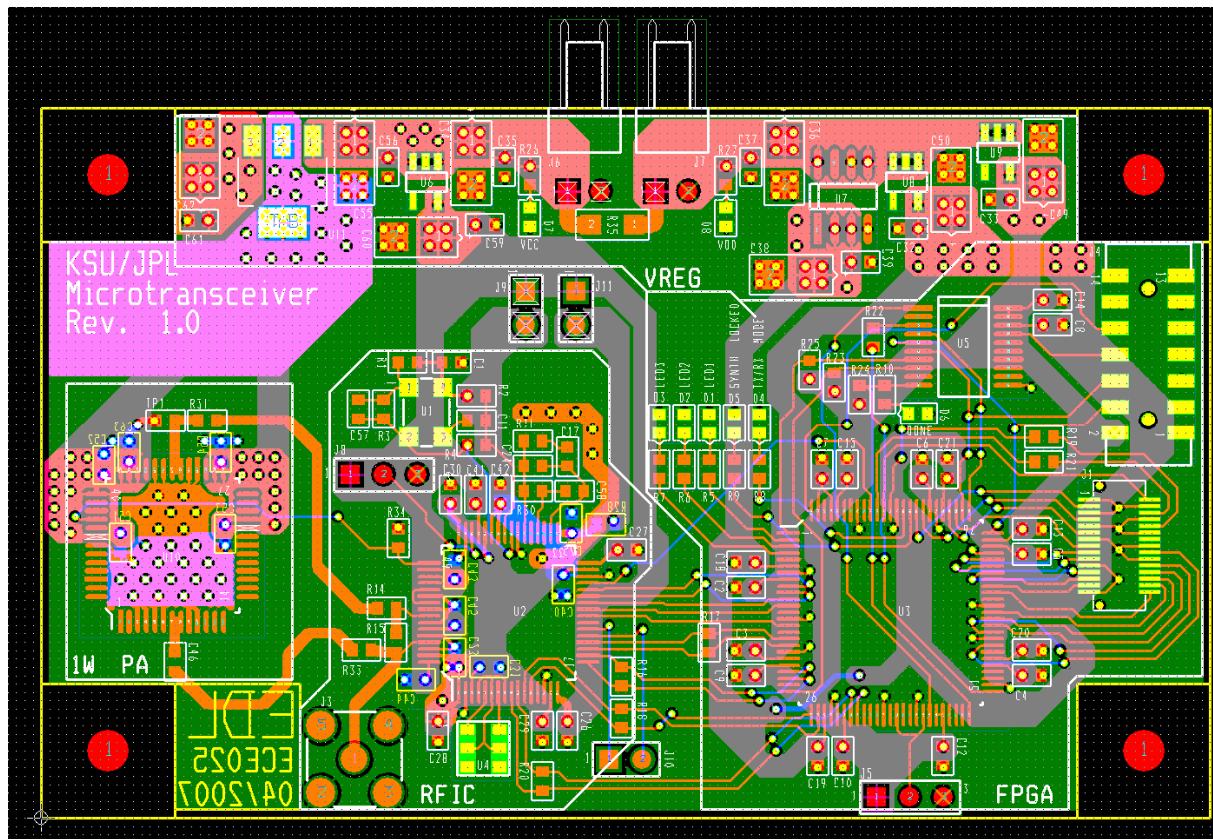
# Evaluation Board with Full Chip Complement



MEP Advanced Technologies NRA 03-OSS-01

Telecommunications and Tracking

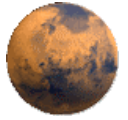
## Developed for evaluation of Micro-transceiver by Mission Planners



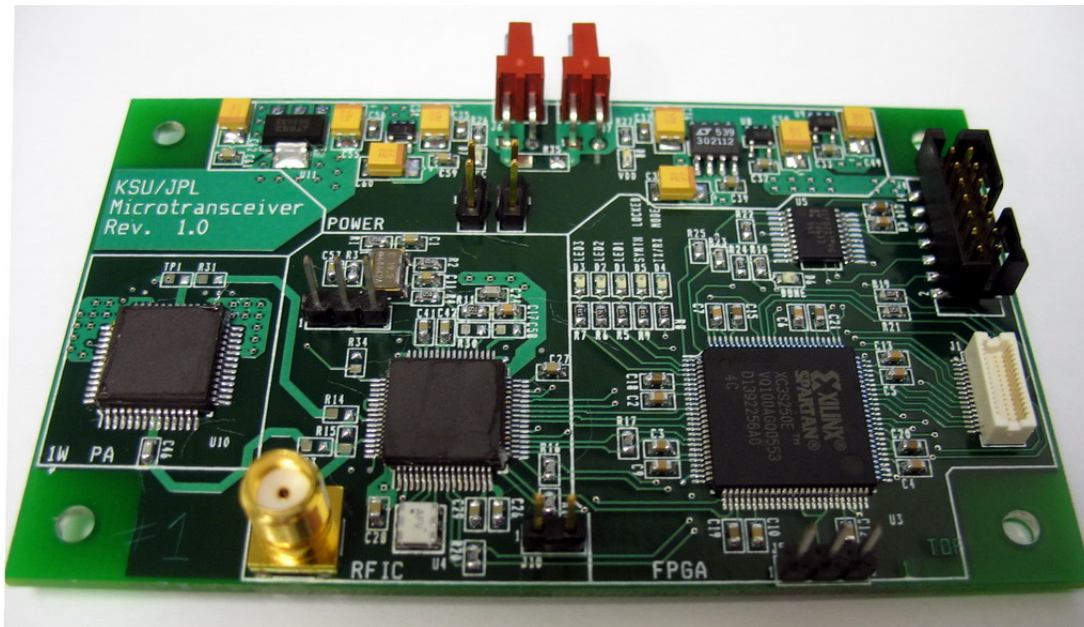
- 4 cm x 6 cm
- 4-layer PCB with internal power and ground for signal integrity
- JTAG programming connector
- LED status lights for testing
- CMOS I/O to host processor on board edge connector
- SMA RF connector to antenna/test-equipment
- On-board regulators for protection of overvoltage



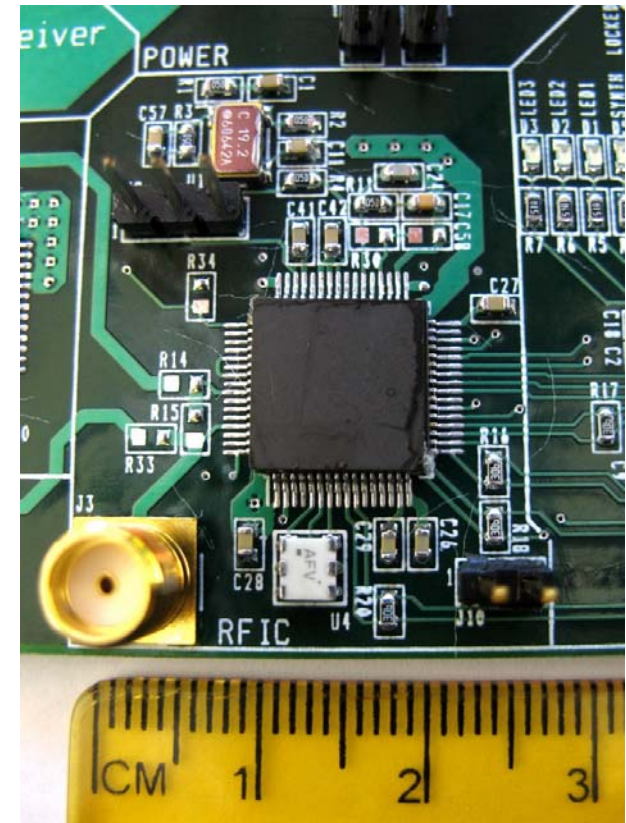
# Evaluation Board Photo and Size



## Full 1-Watt Eval-Board



## RFIC Portion

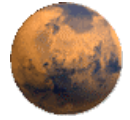








# Commercial Offerings at End of Project



## High Performance Narrowband ISM Transceiver IC

Preliminary Technical Data

ADF7021

### FEATURES

- Low power, low IF transceiver
- Frequency bands
  - 80 MHz to 650 MHz
  - 862 MHz to 940 MHz
- Modulation schemes
  - 2FSK, 3FSK, 4FSK
- Spectral shaping
  - Gaussian and raised-cosine filtering
- Data rates supported
  - 0.05 kbps to 25 kbps
- 2.3 V to 3.6 V power supply
- Programmable output power
  - 16 dBm to +13 dBm in 63 steps
- Automatic PA ramp control
- Receiver sensitivity
  - 125 dBm at 1 kbps, 2 FSK
- On-chip VCO and fractional-N PLL

- On-chip 7-bit ADC and temperature sensor
- Fully automatic frequency control loop (AFC)
- Digital RSSI
- Integrated Tx/Rx switch
- Leakage current <1  $\mu$ A in power-down mode

### APPLICATIONS

- Narrow-band standards
  - ETSI EN 300-220, FCC Part 90, FCC Part 15, FCC Part 95, ARIB STD-T67
- Low cost, wireless data transfer
- Remote control/security systems
- Wireless metering
- Private mobile radio
- Wireless medical telemetry service (WMTS)
- Keyless entry
- Home automation
- Process and building control
- Pagers

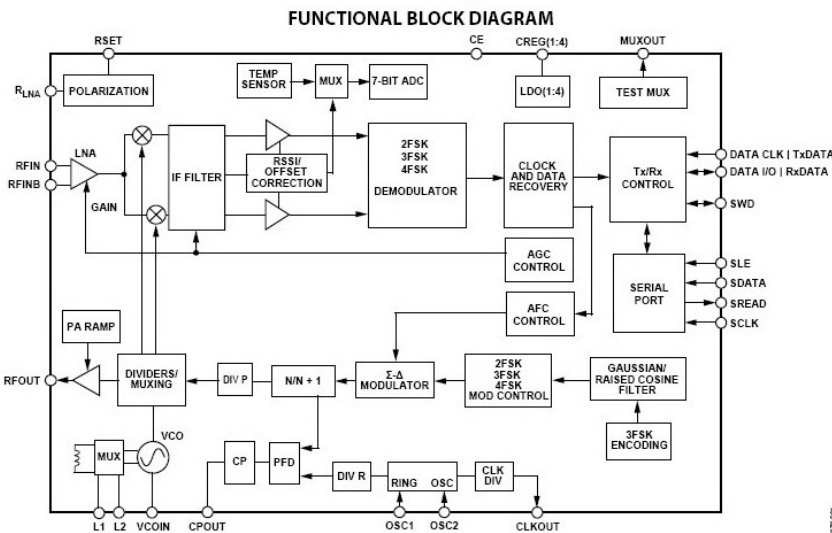


Figure 1.

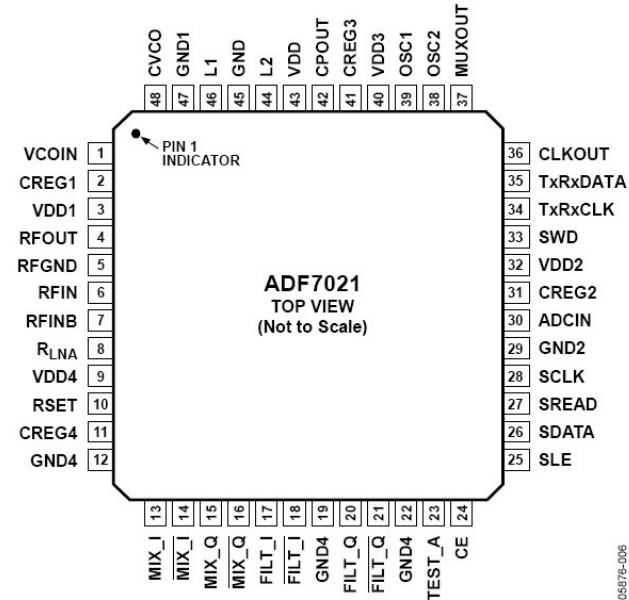


Figure 10. Pin Configuration

- Sensitivity to -123 dBm
- Full on-chip frac-N synthesizer
- No T/R switch
- <+13 dBm versus +20 to +30 dBm RF output
- Not designed for cryogenic temperature
- Not Rad-Hard
- Not Prox-1 Compatible





# To Learn More...



**A Proximity Microtransceiver for Interoperable Mars Communications**

**Project Overview**

**Missions to Mars**

NASA's goals for Mars exploration include "to follow the water" to determine where to look for past or present life, plus a host of studies of the planet's history and current environment. These tasks were started with early missions such as *Mars*, and continue today with the *Spirit* and *Opportunity* rovers as well as through the watchful eyes of orbiters like *Mars Global Surveyor*, *Mars Odyssey*, *Mars Express*, and most recently the *Mars Reconnaissance Orbiter (MRO)*. However, much more of the planet needs to be explored before complex missions like sample return, and ultimately human presence, are undertaken. The UHF micro-transceiver documented in these pages provides an enabling technology for significant expansion of the planetary search.

**Microtransceiver Overview**

Our work is being conducted to support future Mars scout missions. The project will miniaturize and reduce power consumption of Mars scout radio electronics by one to two orders of magnitude. While current transceivers measure as much as 2000 cm<sup>3</sup>, weigh up to 2 kg (on earth), and consume as much as 70 Watts of power, the micro-transceiver will occupy only a few square inches of PC board space (early prototype shown here) and consume as little as 100 mW. This opens the door for sending multiple small assets in a single launch for more extensive exploration, and for developing aerobots, balloons, and networked lander craft. Kansas State University's Department of Electrical and Computer Engineering is partnered with Calspan's Jet Propulsion Laboratory and with Peregrine Semiconductor in this effort. K-State's role is to deliver the radio frequency (RF) circuit portions of the Micro-transceiver, while JPL provides the digital IC, and Peregrine Semiconductor provides the radiation-hardened Silicon-on-Sapphire fabrication expertise.

**Developed for the Martian Environment**

Mars is much colder than Earth due to its added distance from the Sun. Average daily temperatures hover around -60 Celsius (-76 F), while nighttime lows dip to as much as -120 C (-184 F). The micro-transceiver is being designed to withstand these extremes so that the

## Public Site

[www.eece.ksu.edu/research/mars](http://www.eece.ksu.edu/research/mars)

## Intended Audience

- General Public / Academics
- Scout Mission Planners
- New Project Personnel

## Contents

- Conference published material
- Photos illustrating product form-factor, testing, etc.
- Links to publicly available on-line documents and sites



# Publications/Presentations



## Published Papers

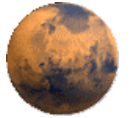
- W. B. Kuhn, M. Mojarradi, and A. Moussessian, “A resonant switch for LNA protection in watt-level CMOS transceivers,” [IEEE Transactions on Microwave Theory and Techniques](#), 2819-25, Sep 2005.
- Yogesh Tugnawat and William Kuhn, “Low Temperature Performance of COTS Electronic Components for Future MARS Missions,” [12<sup>th</sup> NASA VLSI Design Symposium](#), Coeur d'Alene, Idaho, October 4-5, 2005
- William Kuhn, Norman Lay, Edwin Grigorian, “A Low-Volume, Low-Mass, Low-Power UHF Proximity Micro-Transceiver for Mars Exploration,” [12<sup>th</sup> NASA VLSI Design Symposium](#), Coeur d'Alene, Idaho, October 4-5, 2005
- William Kuhn, Norman Lay, Edwin Grigorian, Dan Nobbe “A UHF Proximity Micro-Transceiver for Mars Exploration,” [2006 IEEE Aerospace Conference](#).
- Yogesh Tugnawat and William Kuhn, “Low Temperature Performance of COTS Electronic Components for Future MARS Missions,” [2006 IEEE Aerospace Conference](#)
- J. Jeon and William Kuhn, “A UHF CMOS Transceiver Front-end with a Resonant TR Switch,” [2007 IEEE RAWCON](#)

## In Preparation

- William Kuhn, Norman Lay, Edwin Grigorian, Dan Nobbe “A Micro-transceiver for UHF Proximity Links including Mars Surface-to-Orbit Applications,” Accepted to special issue on [Proceedings of IEEE](#).



# Acknowledgements



- Igor Kuperman, JPL
- Yogesh Tugnawat, K-State MSEE graduate
- Xin He, K-State PhD graduate
- Jeongmin Jeon, K-State PhD student
- Kai Wong, K-State MSEE graduate
- Mark Hartter, K-State MSEE graduate
- Evan Cullens, K-State undergrad
- Keith Kovala, K-State undergrad
- Jack Harder, K-State undergrad