A UHF CMOS Transceiver Front-end with a Resonant TR Switch

Jeongmin Jeon, *Student Member, IEEE* and William B. Kuhn, *Senior Member, IEEE*
Kansas State University, Manhattan, KS, 66502, U.S.A.

***Abstract* — A fully-integrated UHF CMOS transceiver with resonant transmit/receive (T/R) switch is reported. The transceiver's power amplifier (PA) and LNA are simultaneously connected to the antenna and isolated from each other by going to high impedances during receive and transmit respectively. A two-stage single-ended PA produces 19 dBm output power and 36 % PAE is measured at 400 MHz. The LNA has 22 dB gain and 3.4 dB noise figure. In transmit mode, the LNA input impedance becomes 1 kΩ, which absorbs only 0.2 dB of the transmitter output power. The PA side provides 300 Ω toward antenna at receive mode in order not to corrupt noise performance. The transceiver power can be increased through an optional second chip that uses the same TR switch techniques. The optional PA produces 29 dBm power at 29 % PAE. The transceiver was implemented as part of a Mars Micro-transceiver development project for future scout missions.**

***Index terms* — CMOS transceivers, switches, power amplifiers, low-noise amplifier (LNA)**

I. INTRODUCTION

The wireless communication industry has experienced continuing growth in the last decade. Saturated market and harsh competition amongst suppliers resulted in demand for more cost-efficient transceivers. The impetus has driven many researchers into focusing on replacing most of RF front-end with relatively cheap CMOS process. Due to the process' low breakdown voltage, the CMOS PA was one of challenging parts but Watt-level CMOS PAs have been reported using output impedance matching network [1] and transformers [2]. However, if a CMOS LNA shares the antenna with a PA, the LNA remains vulnerable to the PA's high voltage output without some kind of filtering or switch mechanism. In this paper, the resonant switch concept in [3] is applied to the LNA and PA to minimize power loss, NF, and voltage breakdown problems associated with traditional switches.

Although stringent wireless standards have limited wide adoption of single-chip CMOS transceivers, some successful commercial products can be found in select applications such as Bluetooth and WLAN. Likewise, our Mars Microtransceiver project [4] offers an environment in which full integration can be achieved. Here, low mass, power, and volume, and good overall link-efficiency are the primary goals. The resonant T/R switch technique offers a solution for half-duplex operation up to 1 Watt and is applied to its UHF CMOS RFIC. This paper describes the design method of the resonant T/R switch, its effects on performance at both modes, and the measured performance of both the PA and LNA.

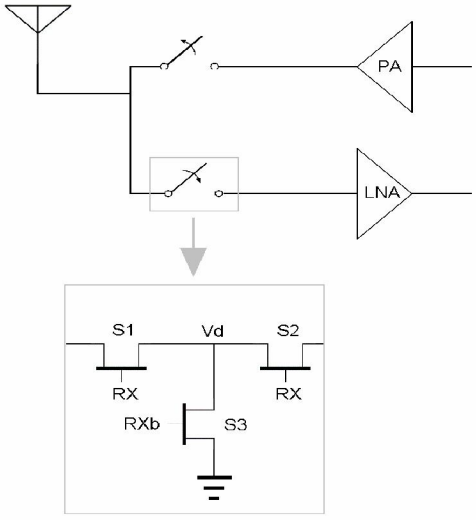


Fig. 1. Traditional T/R switch

II. BACKGROUND AND ANALYSIS

Although a time-division duplexing (TDD) system and a half-duplexing system can eliminate a bulky duplexer filter, they need switches along the path from antenna to RF front-end. Traditional GaAs switch shown in fig. 1 isolates the PA and the LNA by non-overlapping control signals. At receive mode RX is high and S1 and S2 connect the LNA and the antenna and RXb opens S3. The switch between the antenna and PA is set in the opposite way, removing the path to the PA. At the transmit mode S1 and S2 open and S3 closes to ground. The method protects the LNA from high voltage PA output by opening the path (S1 and S2) and effectively grounding Vd (S3). However, S1 and S2 involve transistor on-resistance loss when closed and degrade PA output and LNA noise performance. In addition, the method cannot be used in typical CMOS processes because S1 has to stand high V_{ds} at transmit mode. A new technique has shown that matching networks and switching functions can be combined in a CMOS LNA [3]. This paper expands the method to the PA and makes a complete T/R switch at RF front-end.

1-4244-0445-2/07/$20.00 ©2007 IEEE

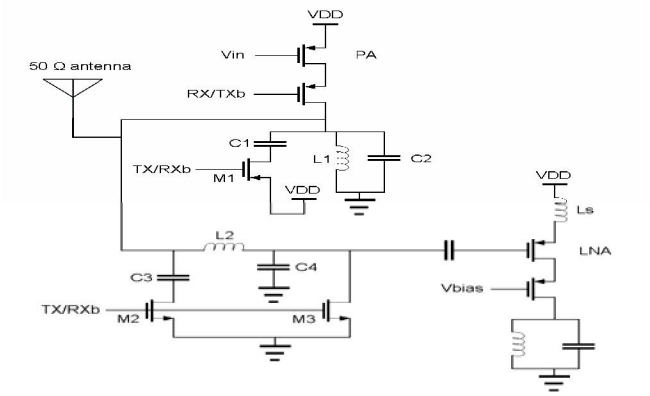


Fig. 2. Proposed T/R switch

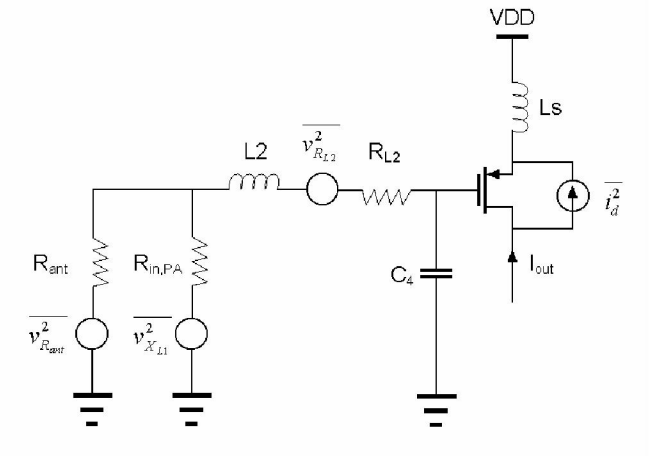


Fig. 3. Noise model of the LNA

The full T/R switch with simple PA and LNA is shown in fig. 2. The half-duplex transceiver operates at 400 MHz and 435 MHz for transmit and receive respectively. The PA has cascoded transistors in order to sustain high voltage at the antenna node without using load resistance transformation. A high efficiency switching mode PA is possible without a RF choke inductor if output reactance is tuned to minimize transistor loss [5]. Inductor L1 together with capacitor C2 in the PA forms parallel resonance for the modified class-E PA mode and maximizes efficiency at transmit mode. At the same time, M2 and M3 close and a parallel resonant circuit is composed of L2 and C3 at the LNA side. If sufficiently high Q inductor is available, $Z_{in,LNA} >> R_{ant}$ and the transmit power loss to the tank is minimized. Suppose that $R_{in,LNA}$ is the effective resistance of the LNA's input in transmit mode. Then loss contributed by the LNA's switch is

$$\frac{P_{loss}}{P_{out}} = \frac{V_{ant}^2 / R_{in,LNA}}{V_{ant}^2 / (R_{in,LNA} \parallel R_{ant})} \quad (1)$$

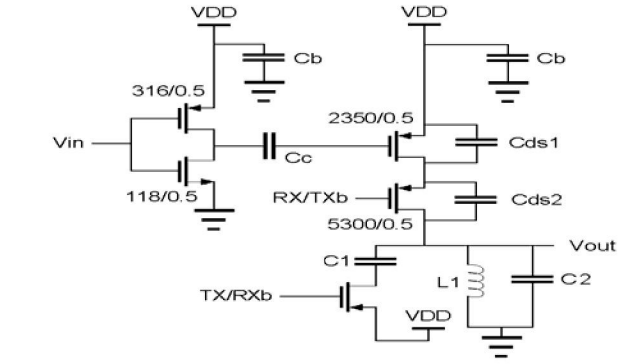


Fig. 4. Power amplifier schematics

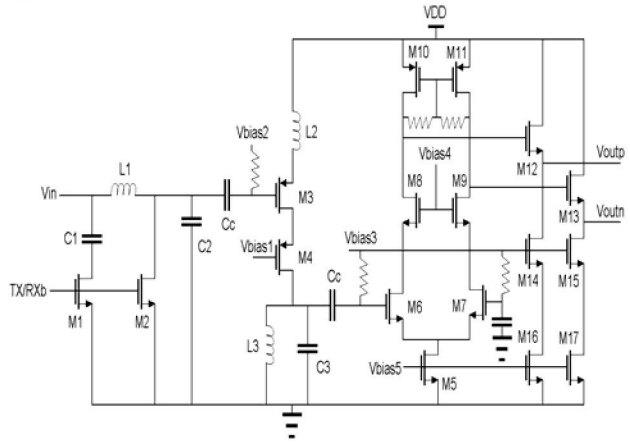


Fig. 5. Low-noise amplifier schematics

Since L2 is fairly large in order to match LNA input to 50 Ω, $R_{in,LNA}$ will be relatively large when it is resonated with C3 during transmit mode and P_{loss}/P_{out} can be held to less than 10 % or 0.5 dB [3].

Inductive source degeneration technique [6] is used for the LNA as shown in fig 2. However, unlike traditional implementations where the goal is a 50 Ohm input to match to a front-end filter, here inductance at the source is chosen to result in a high input resistance at the PMOS gate and it is matched to the source resistance by L2-C4 L-type impedance step-up network. Series resistance in Ls can be neglected if Ls has high Q and total noise output power density is contributed by R_{ant}, $R_{out,PA}$, series resistance R_{L2} in L2, and MOS channel current noise. The noise factor of the circuit can be analyzed from the noise model in fig. 3 [6] as

$$F = \frac{Total\ \ output\ \ noise}{Total\ \ output\ \ noise\ \ due\ \ to\ \ the\ \ source}$$

$$= \frac{S_{no,R_{ant}} + S_{no,R_{out,PA}} + S_{no,R_{L2}} + S_{no,i_d}}{S_{no,R_{ant}}} \quad (2)$$

The addition of $R_{out,PA}$ in parallel with R_{ant} does not change the total output noise due to the source significantly, but the

total output noise increases by $S_{no,Rout,PA}$. Therefore, to avoid degradation of the LNA noise factor, the effects of $R_{out,PA}$ must be minimized and high Q parallel resonance at the PA output is required.

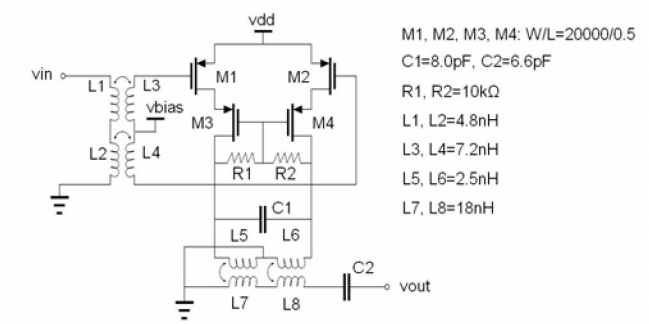


Fig. 6. The 29 dBm optional PA schematic

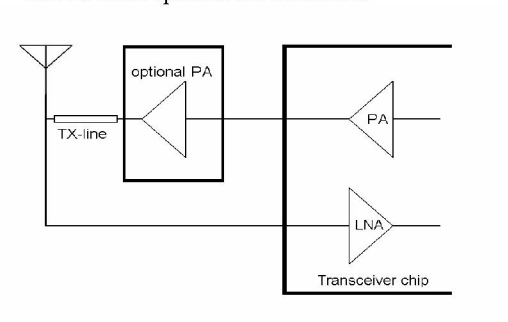


Fig. 7. The transceiver with high output option

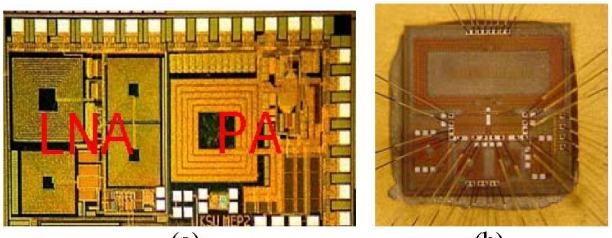
III. IMPLELMENTAION

The transceiver with T/R switch and the optional PA are implemented in 3.3V Peregrine CMOS SOI process on separate chips. The schematics of the transceiver chip's PA is shown fig 4. The first stage is an inverter to generate fast switching input to the second stage. The PMOS transistors are cascoded in the second stage. The PMOS has higher breakdown voltage than NMOS in this process. Thus, it can tolerate safely more than 20 dBm output power at drain. The PMOS is also a lower channel noise source [7] so it adds less noise to the LNA when it is shut down. Taking advantage of thick top metal layer, L1's inductance and Q are approximately 15 nH and 13. At transmit mode L1, C2 and parasitic capacitance C_{ds1} and C_{ds2} form output tuning. The size of L1 is decided initially for class-E operation then load-pull simulation is carried out to find optimum efficiency point. Since the output network is inductive for soft switching, C1 should be added to the circuit at receive mode even though receive frequency is higher than transmit frequency. The LNA is also designed on the transceiver chip (fig. 5). Inductive source degeneration and L-section network match the LNA to 50 Ω input. Cascoding transistors increases voltage gain and makes circuit more stable by isolating input and output. L3-C3 tank boosts voltage swing before gain stage. On-chip spiral inductors are used for L1, L2, and L3. Their specifications are 80nH (Q=10), 72nH (Q=7) and 220nH (Q=5) respectively. Two 18-turn spiral inductors are series-connected to make L3 so its Q is lower than others. The gain stage is a cascoded differential amplifier with active load M10 and M11. It adds not only signal gain and but also converts single-ended signal to differential signal. Buffer stages are followed.

The optional PA is fully integrated on a separate chip. The PA uses cascoded differential structure to prevent drain-source breakdown. On-chip balun interfaces the transceiver chip's single-ended output PA and the optional PA and 1:3 turn ratio transformer/balun at the output enables high output power with 50 Ω load (fig. 6). For high transmit power application the optional PA can be cascaded with the transceiver chip as shown in fig. 7. In this case, microstrip transmission line substitutes for the on-chip resonance circuit and the antenna and LNA see high impedance toward the optional PA at receive mode.

IV. MEASUREMENT

The die photo of the transceiver is shown in fig. 8 (a). The size of the die is 1.5×3.0 mm^2. The transceiver was packaged and tested on the FR4 PCB board. The transceiver's PA delivers 19 dBm to 50 Ω load at the 10 dBm input and PAE is approximately 36 %. The measurement shows that PAE peaks at 9 dBm input (fig. 9 (a)). S11 of the PA at receive mode is 300 Ω (fig. 9 (b)). Measured LNA S21 gain is 22 dB with -50 dBm input (fig. 10 (a)). Hot/cold noise measurement method was used and NF was 3.4 dB at room temperature. 1-dB compression point is -40 dBm. The LNA draws 2.5 mA at the 3.3V power supply excluding 50 Ω output buffer used in testing. S11 at transmit mode is shown in figure 10 (b). The measured S11 is 1 KΩ and it is equivalent to less than 5 % (0.25 dB) transmit power loss from (1). The die photo of the bonded optional PA is shown in fig. 8 (b). An off-chip surface mount capacitor is used in series with C2 at the PA's output for the best efficiency. When the optional PA was driven by the transceiver, 29 dBm output was measured with 29 % PAE. The output impedance toward the optional PA could be up to 360 Ohms after transmission line delay is added resulting in approximate 0.4 dB NF degradation.



(a) (b)

Fig. 8. Die photos of (a) the transceiver (b) the optional PA

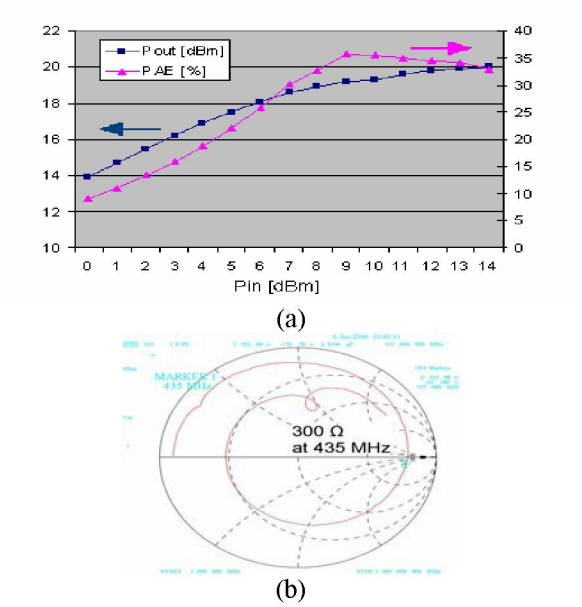


Fig. 9. The transceiver's PA measurement (a) Pout and PAE at transmit mode (b) S11 at receive mode

V. CONCLUSION

Using various processes for each transceiver part raises the total cost and increases size and mass. In recent years researchers have demonstrated that highly efficient Watt-level PA could be realized in economic CMOS process. However, the high output power from the PA is steered by separate GaAs switches to protect the LNA input gate. This paper shows that the resonant T/R switch isolates the LNA from the PA without significant performance tradeoff at RF front-end. The PA in the transceiver generates 19 dBm output with 36 % PAE and the LNA has 3.4 dB NF and 22 dB gain. The resonant T/R switch keeps the LNA from the PA's high voltage output at transmit mode and sacrifices less than 5 % of the transmit power presenting 1 KΩ to antenna. At receive mode the PA provides 300 Ω to antenna resulting in less than 0.5 dB NF degradation. The optional PA for high transmit power application is driven by the transceiver chip and 29 dBm output and 29 % PAE are measured. The design is well suited where a low-volume/power application is needed and is applied to the Mars Microtransceiver development project for future scout missions.

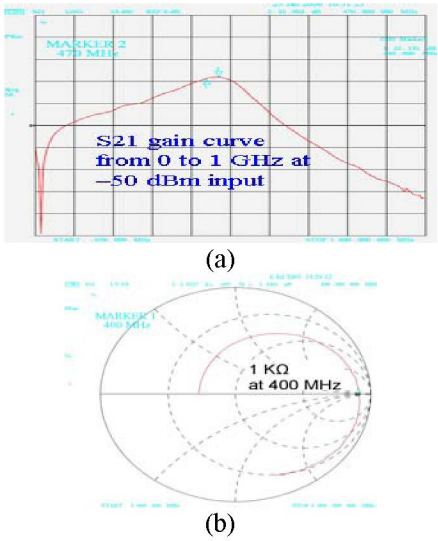


Fig. 10. LNA measurement (a) gain at receive mode (b) S11 at transmit mode

ACKNOWLEDGMENT

This work was supported by the Mars Technology Program of the Jet Propulsion Laboratory, California Institute of Technology under a contract with the National Aeronautics and Space Administration. The authors also gratefully acknowledge the work of the following individuals who have assisted in the design, layout, and testing process: Dan Nobbe, Yogesh Tugnawat, Xin He, Mark Hartter, Kai Wong, Evan Cullens, Keith Kovala, and Jack Harder.

REFERENCES

[1] C. Fallesen, and P. Asbeck, "A 1W CMOS power amplifier for GSM-1800 with 55 % PAE," *IEEE MTT-S international microwave symposium digest*, vol. 2, pp. 911-914 May 2001.

[2] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Fully integrated CMOS power amplifier design using the distributed active-transformer architecture," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 371-383, Mar. 2002.

[3] W. B. Kuhn, M. M. Mojarradi, and A. Moussessian, "A resonant switch for LNA protection in Watt-level CMOS transceivers," *IEEE Transactions on microwave theory and techniques*, vol. 53, issue. 9, pp. 2819-2825, Sep. 2005.

[4] Kuhn, W., Lay, N., and Grigorian, E., "A UHF Proximity Micro-Transceiver for Mars Exploration," IEEE Aerospace Conference, 04-11 March 2006.

[5] D. K. Choi and S. I. Long, "Finite DC feed inductor in class E power amplifier – a simplified approach," *IEEE MTT-S international microwave symposium digest*, vol. 3, pp. 1643-1646 Jun. 02.

[6] D. K. Shaefferm and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745-759, May 1997.

[7] A. W. Orsborn, *Noise analysis and automatic tuning of Q-enhanced LC bandpass filters*, M.S. thesis Manhattan, KS: Dept. Electr. Comput. Eng., Kansas State Univ., 2001.