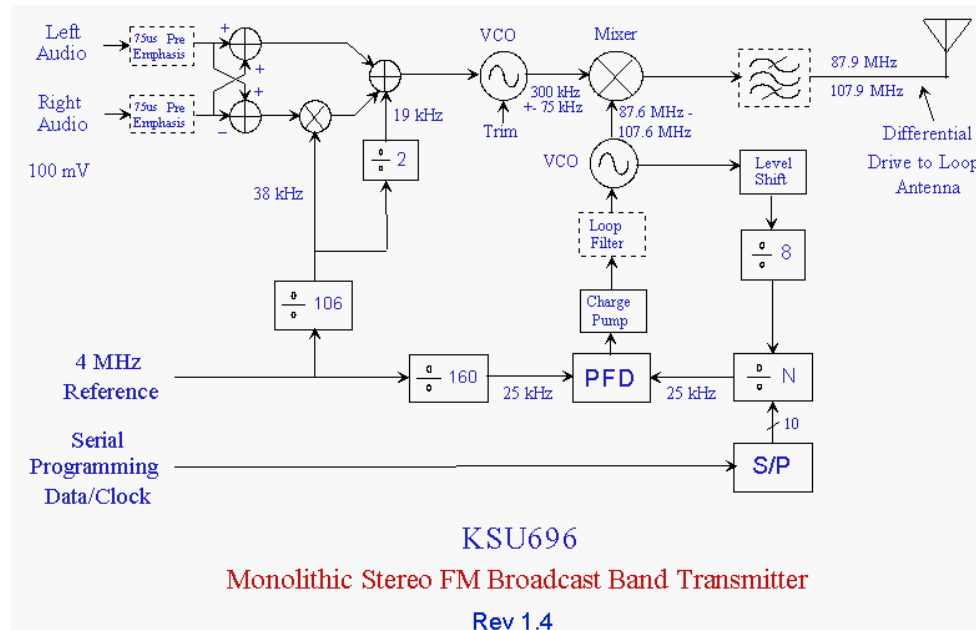


Monolithic Stereo FM Broadcast Band Transmitter
EECE 696 – Integrated Circuit Design
Kansas State University
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Alpha-Bits Semiconductors Testing Results for MOSIS
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Project Description

The class was divided into two companies: Alpha-Bits Semiconductors and Beta-Tronix. This report is for the Alpha-Bits Semiconductors design. Each company was responsible for the design, simulation and layout of a prototype of the product. Two different prototypes were sent to MOSIS for fabrication, and the testing of each prototype is described in this report. Design and layout information for this chip may be found on our web page at <http://www.eece.ksu.edu/~eece696/alpha/alpha.htm>. Included in this web page are operation and design descriptions, detailed schematics, simulation results and layout images.



Design Overview

The product is a prototype of a monolithic stereo FM broadcast band transmitter. The AMI ABN 1.5µm scalable CMOS process was used with a lambda of 0.6µm.

The input to the chip is a stereo audio signal approximately 100mV in amplitude, that has been preemphasized and is AC coupled to the input pins. To enable stereo transmission, a matrix of two-input summing amplifiers is used to create a left-plus-right channel and a left-minus-right channel. The left-minus-right signal is upconverted to a center frequency of 38kHz. The resulting signal is fed into a three-input summing amplifier along with the left-plus-right signal and a 19kHz-clock signal (which is used as a pilot tone in demodulation). A 38kHz clock is created from passing a 4MHz reference clock signal

(located off-chip) through a divide-by-106 counter. Passing the 38kHz clock through a divide-by-2 counter creates the 19kHz clock.

The output of the three-input summing amplifier is fed to a low frequency voltage-controlled oscillator (LFVCO) with a center frequency of 300kHz. The LFVCO varies between 225 and 375kHz, creating a 150kHz channel.

The output of the LFVCO is fed into a mixer along with an output from the high-frequency VCO (HFVCO). The mixer upconverts the output of the LFVCO to the broadcast band of 87.6MHz to 107.6MHz. The HFVCO is part of a phase locked loop (PLL). To start the PLL the output of the HFVCO is sent through a level-shifter. The output of the level shifter is passed through a divide-by-eight counter. The signal is then passed through a divide-by-N counter, which divides the signal so that the output has a center frequency of 25kHz. The serial programming data, which comes from an off-chip source, determines the number N. This data is fed into a 10-bit serial-to-parallel converter, which is input into the divide-by-N counter. This data determines the center frequency of the broadcast band.

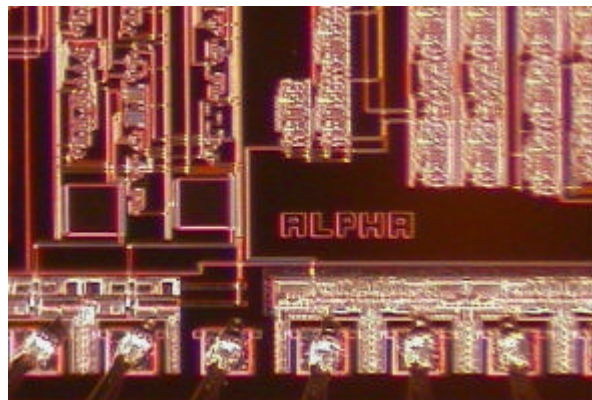
The output of the divide-by-N counter is one of the inputs into a phase-frequency detector (PFD). The other input to the PFD is the output of a divide-by-160 counter. The input to the divide-by-160 counter is a 4MHz frequency reference located off-chip. The PFD compares the phase and frequency of the output of the divide-by-106 and divide-by-N counters and sends their difference to a charge pump. The output of the charge pump is then passed through a loop filter (located off-chip) and into the input of the HFVCO, completing the PLL.

Simulation and Layout Information

This design was simulated with Spice3f5 using the BSIM3 version 3.1 models at the four process corners over a temperature range of -20°C to 70°C . The layout was performed with Magic version 6.4.4 and converted to CIF format for submission to MOSIS.

Test Equipment

A Wavetek 810 was used for signal generation and clock references. A Hewlett-Packard 6236B was used for the power supply and trim voltages. The DC levels were measured with a Hewlett-Packard 3466A digital multimeter. A Fluke PM3392A oscilloscope was used for measurement of analog and digital signals. A Hewlett-Packard 4195A Network/Spectrum Analyzer was used for observation of signals also.



Close-up of the Alpha-Bits Semiconductor's Chip

Alpha-Bits Semiconductors' Test Results

Summing Amplifiers and Low Frequency Mixer

The summing amplifiers have two differential inputs which are called the left and right channels. To test the circuits a 500mV, 1kHz signal was input into the left audio channel with the right audio channel grounded, and 100 μ F AC coupling capacitors are used for all inputs.

The bias points for the positive and negative inputs of the left channel were measured as 2.8V, close to the design value. The positive input for the right channel had a 2.8V bias, but the negative right input was 4.2V, which is higher than expected. The reason for this discrepancy is unknown, due to lack of internal probe points. The bias point of the output was measured at 1.1V as seen through a source-follower pad-driver/buffer, somewhat lower than the expected value of 1.5V. The three input-summing amplifier had no signal where a 500mV signal was expected. The cause of this problem is currently unknown, due to lack of internal probe points. In addition, no 38kHz or 19kHz signals were present in the output because the divide-by-106 counter is not operational, due to a layout error in the static divide-by-two cell used (see digital section below). The input resistance for the left channel is 83k Ω , and the input resistance to the right channel is 107k Ω . They are designed to be 100k Ω , so each is in the 20% tolerance for n-well resistors.

Digital

The divide-by-106, divide-by-160 and divide-by-N counters are not operational despite extensive layout versus schematic checks. The error occurred during the final integration when a static D-flip-flop subcell in the digital layout was changed without renaming the subcell. An older version of the subcell was used under the same name in the final layout, and so a version of the flip-flop was overwritten. The newer version has different dimensions and is therefore not compatible with the older version, causing the circuit to have incomplete connections.

LFVCO

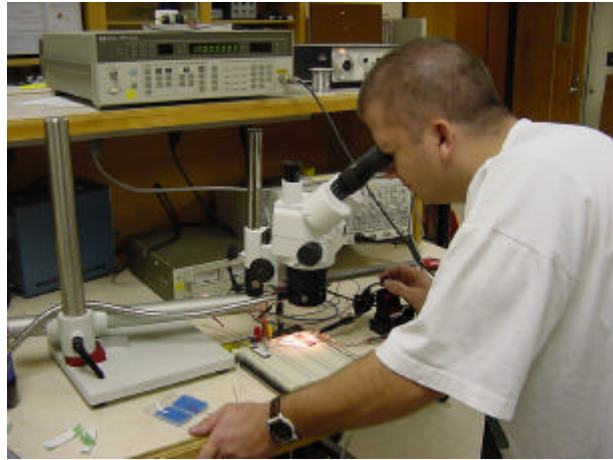
The LFVCO is operational, and has an output frequency of 555kHz. An increase in the frequency trim voltage caused the output frequency to increase as designed. A design error did not allow for a decrease in the frequency output so it could not be adjusted to the desired frequency of 300kHz.

HFVCO

The output was tested with and without external 0.01 μ F capacitors, which were used to stabilize the common-mode feedback loop. A control voltage was applied to a pin to simulate the output of the loop filter. Unfortunately, there was no signal present at the output for any voltage applied to its input.

Probing internal pads at the output of the HFVCO was done to see if the buffer between the output of the HFVCO and the bondpad was causing the signal to be cut off, but there was no signal present at these probe points either. The problem was traced to an error in layout which the Magic extraction tools could not detect (Nwell resistors extract as shorts and must be manually edited in the extract file.) The HF mixer has its two input resistors connected in such a way that the HFVCO sees a low resistance in parallel with its' output.

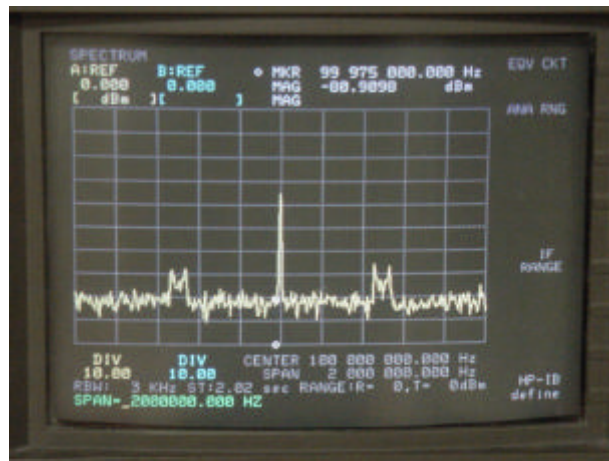
This combines with the resistor in the HFVCO in parallel and results in an equivalent resistance that is lower than the value needed for the HFVCO to oscillate.



Probing the HFVCO

High Frequency Mixer

To test the HF mixer an analog signal was input into the LFVCO control, which creates an FM signal with a center frequency of about 1MHz. A 100 MHz signal was then injected into the other input of the HF mixer via a probe, substituting for the non-functional HFVCO. The HF mixer correctly upconverted the FM signal to center frequencies of about 101 MHz and 99 MHz.



Output spectrum of transmitter with external HF carrier injected through probe point.

Buffer

Some analog test points that are output to a pin used a common buffer to prevent the pad from loading down the circuits. The buffer was a two stage source-follower configuration. The buffer had too large of a width-to-length-ratio increase between the two stages creating a loading on the first stage of the buffer. The consequence was a cutoff frequency of about 1MHz. This causes attenuation to the signals input to the buffer.

Conclusions

The lack of internal test points prevents us from individually testing the divide-by-2 counter, divide-by-eight counter, low-frequency mixer, two and three-input summing amplifiers, phase-frequency detector and charge pump. Instead these circuits are tested in conjunction with other parts and so it becomes more difficult to pinpoint any problems in the circuit. More internal test points for bias points and current references would aid the testing of this chip. Since this lack of internal probe points limited the testing of this chip, future versions of this chip will include more test points. To aid in this, our university has purchased some Picoprobes for the internal test points.