
A MONOLITHIC STEREO FM BROADCAST BAND TRANSMITTER

EECE 690 - VLSI ASIC Development Final Paper

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1 Background

1.1 EECE 696 - Integrated Circuit Design Course

As a part of the curriculum at Kansas State University, the Integrated Circuit Design course gives students enrolled a chance to design and fabricate an IC of their own. In the Fall 1999 IC Design Course, the goal was to put a complete system on a chip. Since this is an introductory course in IC design, the basics of fabrication processes, device theory, layout tools and techniques must be taught along with analog and digital IC design. This subject material consumes roughly half of the semester, while the remaining half is spent on a class project. Students must complete the design, simulation, layout and LVS checks in the remaining half of the semester in order to meet grading and tapeout deadlines.

For the project, the class was divided into two teams (referred to as Alpha-Bits Semiconductors and Beta-Tronix). Each team was made up of analog, digital, radio-frequency and test engineers (who actually performed final system layout duties). The project goal and system specifications were identical for each team, and the information given in the class lectures enabled the students to design their portions of the project. At the end of the Fall 1999 semester the students published their work on the web (this can be seen at www.eece.ksu.edu/~eece696), which served as the final technical report for the project. Each team submitted a complete layout that was then readied for tape out. Kansas State University does not have an in-house fabrication service, so the MOSIS (www.mosis.org) service was used to get the chips manufactured.

1.2 EECE 690 - VLSI ASIC Development Course

After the IC Design course is finished, the students either graduate or continue with other coursework. This presents obvious difficulties in adequately testing and developing the chips after they are received from MOSIS, since the chips are received a few months after the completion of the course. An opportunity for further learning exists with the untested chip and with some testing and development, a push toward a finished product can be made.

The purpose of the VLSI ASIC Development course is to continue the IC Design project so that a student can gain experience with the processes involved with developing a product. One benefit of this course is that student will gain a view of the system beyond the section that he or she was involved with in the original project. The student is exposed to testing methods for ICs, gains circuit level design experience with the modifications made to the chip, and gains further experience with simulation and layout tools. The student is also able to evaluate the work done in the previous class and possibly propose changes for future offerings of the IC Design course.

2 Objectives of EECE 690 VLSI ASIC Development Course

The initial offering of the VLSI ASIC Design course was given as an independent study, 8 week course in the Summer 2000 semester. The objectives of the course were the following (some objectives were addressed in parallel):

1. Thoroughly test the chips developed in EECE 696, troubleshoot problems, and write test reports for MOSIS
2. Evaluate test results and plan the modification of the design
3. Design and simulate the subcircuits that need to be modified
4. Layout and perform LVS checks, send off for fabrication by MOSIS
5. Submit final documentation, write report and make available via the world wide web

3 IC Design Course Project Description

The EECE 696 project goal was to design a prototype of a monolithic stereo FM broadcast band transmitter as illustrated in Figure 1. The AMI ABN scalable CMOS process was used with a lambda of $0.6\mu m$ giving a minimum channel length of $1.2\mu m$.

The input to the chip is a stereo audio signal approximately 100mV in amplitude, that has been preemphasized and is AC coupled to the input pins. To enable stereo transmission, a matrix of two-input summing amplifiers is used to create a left-plus-right channel and a left-minus-right channel. The left-minus-right signal is upconverted to a center frequency of 38kHz. The resulting signal is fed into a three-input summing amplifier along with the left-plus-right signal and a 19kHz-clock signal (which is used as a pilot tone in demodulation). The 38kHz clock is created from passing a 4MHz reference clock signal (located off-chip) through a divide-by-106 counter. Passing the 38kHz clock through a divide-by-2 counter creates the 19kHz clock.

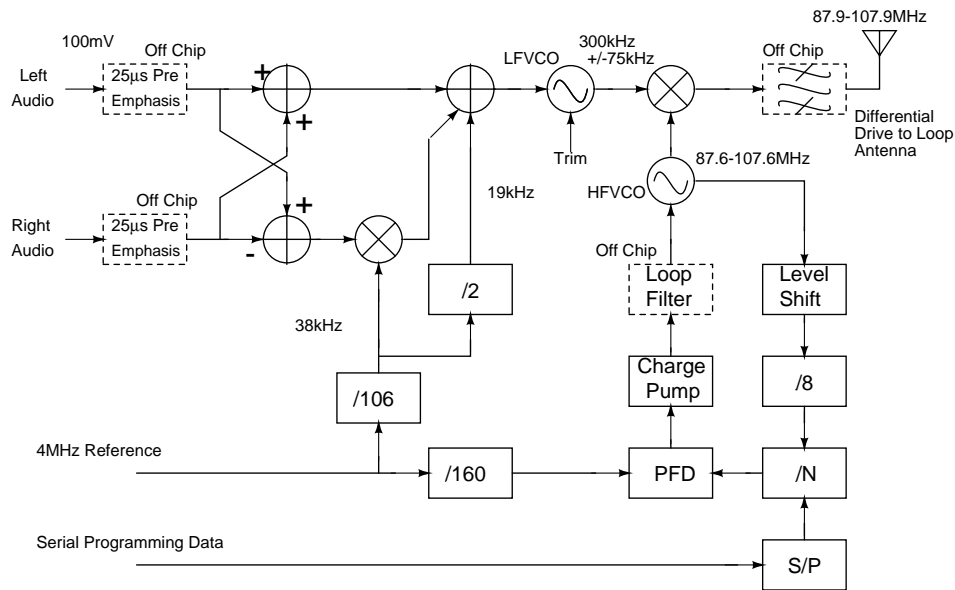


Figure 1: Block diagram of the KSU696

The output of the three-input summing amplifier is fed to a low frequency voltage-controlled oscillator (LFVCO) with a center frequency of 300kHz. The LFVCO varies between 225 and 375kHz, creating a 150kHz channel.

The output of the LFVCO is fed into a mixer along with an output from the high-frequency VCO (HFVCO). The mixer upconverts the output of the LFVCO to the broadcast band of 87.6MHz to 107.6MHz. The HFVCO is part of a phase

locked loop (PLL). To start the PLL the output of the HFVCO is sent through a level-shifter. The output of the level shifter is passed through a divide-by-eight counter. The signal is then passed through a divide-by-N counter, which divides the signal so that the output has a center frequency of 25kHz. The serial programming data, which comes from an off-chip source, determines the number N. This data is fed into a 10-bit serial-to-parallel converter, which is input into the divide-by-N counter. This data determines the center frequency of the transmitted signal in the broadcast band.

The output of the divide-by-N counter is one of the inputs into a phase-frequency detector (PFD). The other input to the PFD is the output of a divide-by-160 counter. The input to the divide-by-160 counter is a 4MHz frequency reference located off-chip. The PFD compares the phase and frequency of the output of the divide-by-106 and divide-by-N counters and sends their difference to a charge pump. The output of the charge pump is then passed through a loop filter (located off-chip) and into the input of the HFVCO, completing the PLL.

4 Testing

The testing took three to four weeks instead of the week that was allotted. A main problem with the testing was that there were not enough internal (on-chip) test points. This made it difficult to pinpoint the problems with the circuits. At the time the layout was performed in the IC Design course, there was a lack of on chip probing equipment available, so adequate preparations were not made for internal chip measurements. At the time of testing, proper probing equipment was available so that the internal test points that did exist were used.

4.1 Alpha-Bits Semiconductors' Test Results

4.1.1 Summing Amplifiers and Low Frequency Mixer

The summing amplifiers have two differential inputs which are called the left and right channels. To test the circuits a 500mV, 1kHz signal was input into the left audio channel with the right audio channel AC grounded, using 100 μ F AC coupling capacitors for all the inputs. The three-input summing amplifier outputs no signal where a 500mV signal is expected. No 38kHz or 19kHz signals were present in the output because the divide-by-106 counter is not operational.

In an effort to debug the analog circuits, bias points were checked where possible. The bias points for the positive and negative inputs of the left channel were expected to be 2.8V. The positive input for the right channel had a 2.8V bias, but the negative right input was 4.2V, which is higher than expected. The bias point of the output was 1.1V. The input resistance for the left channel was 83k Ω , and the input resistance to the right channel was 107k Ω They are designed to be 100k Ω , so each is in the 20% tolerance for n-well resistors. Further debugging was not possible due to a lack of on-chip test points in this portion of the system.

4.1.2 LFVCO

The LFVCO was operational, and had an output frequency of 555kHz. As the frequency trim voltage was increased, the output frequency increased as designed. However, the design did not allow for a decrease in the output frequency so it could not be adjusted to the desired frequency of 300kHz.

4.1.3 HFVCO

The HFVCO was tested with and without external $0.01\mu\text{F}$ capacitors, which are used to stabilize the common-mode feedback loops. A control voltage was applied to a pin to simulate the output of the loop filter. There was no signal present at the output for any voltage applied to its input. The desired frequency range of the output is 87.6MHz to 107.6MHz.

Probing internal pads at the output of the HFVCO was done to see if the buffer between the output of the HFVCO and the bondpad was causing the signal to be cut off, but there was no signal present at these probe points either. Further tests revealed that the HF mixer had its two input resistors connected in such a way that the HFVCO saw a low resistance in parallel with its output. This combined in parallel with the resistor in the HFVCO and resulted in an equivalent resistance that was lower than the value allowed for the HFVCO to oscillate.

4.1.4 High Frequency Mixer

To test the HF mixer an analog signal was input into the LFVCO, which then output a FM signal with a center frequency of about 1MHz. A 100 MHz signal was then injected into the other input of the HF mixer via a probe. The HF mixer correctly upconverted the FM signal to center frequencies of about 101 MHz and 99 MHz, so the HF mixer was operational. However, there was a problem with the two $5\text{k}\Omega$ nwell resistors at the mixer's input. The nwell regions for these resistors expanded when the layout was converted to a cif file. This expansion was in accordance with the layout rules the Magic layout tool uses when nwell regions are too small and close together. This does not prevent the mixer from correct operation, but it significantly changes its' the resistance that the HFVCO sees.

4.1.5 Digital

The divide-by-106, divide-by-160 and divide-by-N counters were not operational despite extensive layout versus schematic checks during the original design. Their inoperability is due to an error that occurred during final integration. During the final layout, a static D-flip-flop subcell used in a section of the digital layout was changed without renaming the subcell. An older version of the subcell used in a different section of the layout had the same name as the newer version, so a version of the flip-flop was overwritten. The newer version has dif-

ferent dimensions and is therefore not compatible with the older version, causing the circuit to have incomplete connections.

4.1.6 Buffer

Some test points that were output to a pin used a common buffer to prevent the pad from loading down the circuits. The buffer was a two-stage source-follower configuration. The buffer had too large of a width-to-length-ratio increase between the two stages which created too much loading on the first stage of the buffer. The consequence was a cutoff frequency of about 1MHz which caused attenuation to the signals input to the buffer

4.2 Beta-Tronix' Test Results

4.2.1 Summing Amplifiers and Low Frequency Mixers

In the Beta-Tronix version of the audio summing amp circuits, the first test point was taken at the output of the LF mixer, which mixes the output of the left-minus-right summing amplifier with a 38kHz clock signal. For a 500mV, 1kHz input to the left channel and no input to the right channel, the mixer output was 500mV as expected. When 500mV was input to the right channel and 500mV to the left channel, nothing was output from the mixer since this is the left minus right channel. When 440mV was input to the left channel and 220mV was input to the right channel, 220mV was output from the summer as expected.

With no input to the left and right channels, a 2MHz clock input (2MHz was used instead of the planned 4MHz because a 4MHz signal generator was not available at the time), and a high signal applied to the clear pin, a 19 kHz signal was output from the two-input summer. This indicates that the divide-by-106 counter is operating correctly.

With signals input into the left channel and a 2MHz clock input, the output of the three input summer contained the input signal mixed with a 19 kHz signal, verifying correct operation of the LF mixer and the three-input summing amplifier. Without any input to the left or right channels there was no 9.5kHz signal observed; there was only a 19kHz signal from the divide-by-106 counter. This is due to the divide-by-2 counter not being connected correctly in the layout. Instead of \overline{Q} being connected to D on the D-flip-flop, Q was connected to D . This caused the output to remain latched to either high or low.

4.2.2 LFVCO

With no trim voltage input, the LFVCO output a 435kHz square wave. As the trim voltage was increased, the frequency of the output decreased. For a trim voltage of 0.5V, a center frequency of 300kHz was output which was the desired frequency output. For an input sinusoid of 540mV peak-to-peak amplitude, the frequency changed by 666kHz, or about 1.2Hz/mV frequency deviation.

4.2.3 HFVCO

With no external capacitors, the HFVCO output an 8MHz signal. This was much less than the desired range of 87.6MHz to 107.6MHz. The common-mode feedback loop was working correctly.

4.2.4 High Frequency Mixer

There was no signal output from the HF mixer. Due to the lack of internal test points, a conclusion to why it did not work could not be made.

4.2.5 Digital

The divide-by-106 counter output 19kHz for a 2MHz clock input and a high signal applied to the clear pin, so the divide-by-106 operation is performing correctly. The divide-by-160 counter output 12.5kHz for a 2MHz clock input and a high signal applied to the clear pin and so it is also performing correctly. The output square waves were sharp with adequately fast rise and fall times. The static flip-flops performed correctly up to a frequency of 70MHz.

Even with a good square wave output from the level shifter in the PLL, the divide-by-eight counter did not produce an intelligible output. The difference between the divide-by-106 and 160 counters and the divide-by-eight counter is that the former use static flip-flops and the latter uses dynamic flip-flops.

4.3 Testing Comments

The lack of internal test points prevented us from individually testing many circuits. Instead these circuits were tested in conjunction with other parts and so it became difficult to pinpoint problems. This significantly increased the amount of time required to adequately test the chips. More internal test points for bias points and current references would aid the troubleshooting of these chips. Since this lack of internal probe points limited the testing of this chip, future versions of the chip should include more test points.

5 Modifications

Since two chips were fabricated and tested, the best parts of each chip could be used, but since the Beta-Tronix chip was mostly operational, it was decided that it would be more efficient to just modify this design instead. It was also decided that image rejection would be added to the high-frequency mixer, and the topology of the HFVCO needed to be changed. Adding on chip preemphasis filters, designing an adequate buffer for off chip test points and adding a charge pump and loop filter to the PLL were planned, but time constraints prevented from accomplishing this with one student in 8 weeks. A block diagram of the modified system is shown in Figure 2.

5.1 HFVCO

It was decided that a different topology of the HFVCO would be tried. The common-mode feedback approach was originally used to stabilize the bias voltage of the transconductor circuits. In order to simplify the design, a new approach to biasing was used to stabilize this voltage instead of the common-mode feedback circuit.

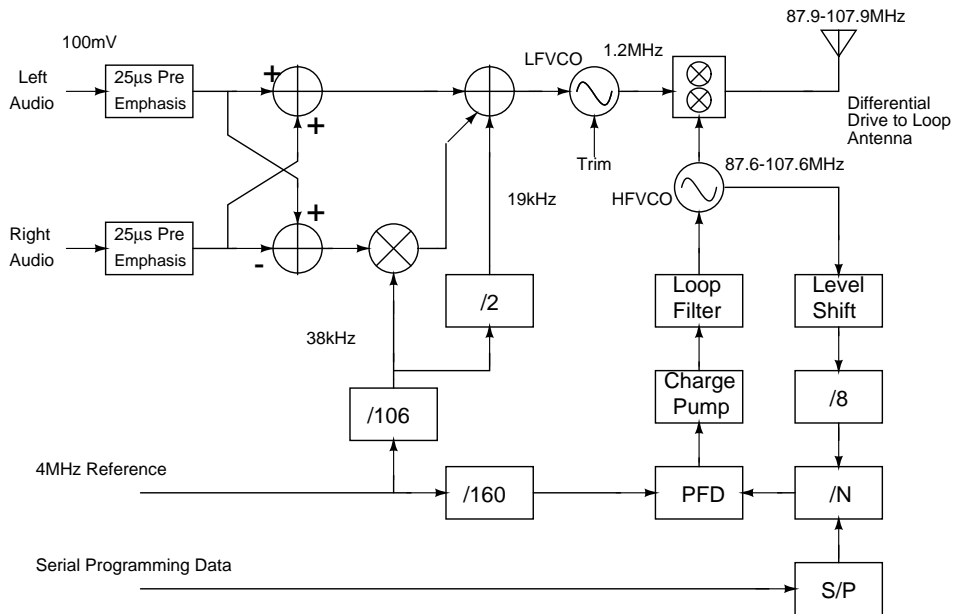


Figure 2: Block diagram of the KSU690

5.2 Image Reject Mixer

In the original design, the mixer did not include image rejection and so it was necessary to use an off chip bandpass filter to eliminate out of band transmissions. In order to reduce the number of external components needed for the chip, it was decided that an image reject mixer could be used to reduce the out of band transmissions in stead of an off-chip bandpass filter. An image reject mixer uses a different circuit topology than the single mixer idea. It uses a two mixers and a combination of phase shift networks to produce an output free of out of band signals.

5.3 LFVCO

A modification to the LFVCO was needed since the 90 degree phase shift for the image reject mixer was implemented with a divide-by-four circuit. Since we used the divide-by-four operation, the nominal frequency of the LFVCO needed to be increased from 300kHz to 1.2MHz. The LFVCO only needed a decrease in the capacitance value that determines the output frequency to achieve this.

6 Design

6.1 HFVCO Design

The G_m -C oscillator topology used is shown in Figure 5. The G_m -C oscillator uses an active inductor instead of a passive inductor because it is difficult to create high-Q inductors on-chip at FM broadcast band frequencies in a standard CMOS process. The active inductor is created by using transconductance amplifiers and an integrating capacitor. How this can be done is shown in Figure 3.

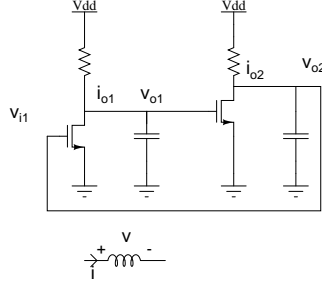


Figure 3: Active Inductor Example

The equation for the current passing through a passive inductor with inductance L with zero initial conditions is:

$$i = \frac{1}{L} \int_0^t v dt$$

For the active inductor a similar relationship can be shown. The output current of the first transconductor is:

$$i_{o1} = g_m v_{i1}$$

The voltage across the integrating capacitor is given by:

$$v_{o1} = \frac{1}{C} \int_0^t i_{o1} dt$$

Since v_{o1} is the input voltage to the second transconductor, the output current of the second transconductor is:

$$i_{o2} = g_m v_{o1}$$

Due to the output of the active inductor being connected to the input, the input voltage v_{i1} can be expressed as:

$$v_{i1} = v_{o2} = \frac{1}{C} \int_0^t i_{o2} dt$$

Substituting for v_{i1} and i_{o2} we have:

$$\frac{i_{o1}}{g_m} = \frac{1}{C} \int_0^t g_m v_{o1} dt$$

Which gives a relationship like the passive inductor:

$$i_{o1} = \frac{g_m^2}{C} \int_0^t v_{o1} dt$$

The inductance value of the active inductor is then given by:

$$L = \frac{C}{g_m^2}$$

This inductance resonates with the capacitor with the aid of a negative resistance cell at a frequency of

$$\omega = \sqrt{LC}$$

Substituting for L gives:

$$f = \frac{g_m}{2\pi C}$$

The value of this frequency is varied by changing i_{o1} . This frequency control is implemented by connecting FETs in parallel to the FETs in the first g_m cell. A voltage is applied to the gates of these parallel-connected FETs from an off-chip source and a change in this voltage causes a change in the output frequency.

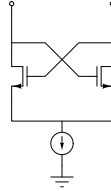


Figure 4: Negative Resistance Cell

The negative resistance cell sees the resistance of the PFETs in the second g_m cell in parallel with the $100\text{k}\Omega$ resistor. This is the resistance that the negative resistance cell must cancel in order for the circuit to resonate. To achieve the negative resistance, two cross coupled FETs are used as shown in Figure 4. A rise in the drain voltage on one FET will cause an increase in the gate voltage of the second FET, which causes the current of the second FET to increase. This increase in current in the second FET causes its' drain voltage to decrease, which in turn causes the gate voltage of the first FET to decrease. This causes a decrease in the current of the first FET which can be thought of as an effective current flowing out of the first FET. This means that on the terminal of the cell

$$\cos(\omega_1 t)\cos(\omega_2 t) = \frac{1}{2}\cos(\omega_2 - \omega_1)t + \frac{1}{2}\cos(\omega_2 + \omega_1)t$$

From this we see that the output of the mixer would have frequency components at the sum and the difference of the input frequencies. For example, if the LFVCO is at 300 kHz and the HFVCO is at 100 MHz, equal level outputs would exist at 99.7 MHz and 100.3 MHz. This effect is not desirable and in fact so it is necessary to use a circuit topology that would prevent the extra component from appearing at the output.

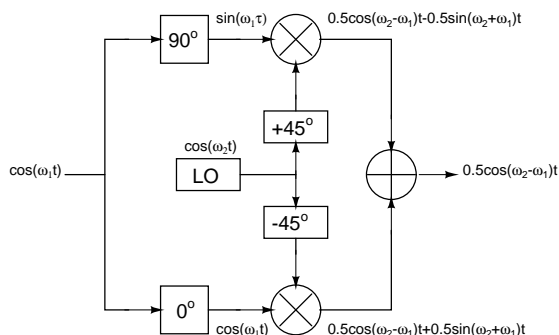


Figure 6: Block diagram of the image reject mixer

Instead of the single mixer used in the EECE 696 design, Figure 6 shows that the topology used in the EECE 690 design mixes two versions of the LFVCO output with two versions of the HFVCO output. The versions of the LFVCO output are phase shifted at 90 degrees and 0 degrees. The versions of the HFVCO output are phase shifted at +45 degrees and -45 degrees. The 90 degree phase shifted signal is mixed with the +45 degree signal and the 0 degree phase shifted signal is mixed with the -45 degree signal. The two resulting products are then summed together to get the final upconverted signal. The resulting signal is centered at the sum of the two output frequencies, while the signal at the difference between the LFVCO and HFVCO is rejected.

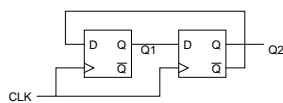


Figure 7: The divide-by-four 90 degree phase shifter

The 90 degree phase shift on the LFVCO input can be done with a divide by four operation. This circuit is easily made with two flip flops as shown in Figure 7. The outputs Q_1 and Q_2 are in quadrature with respect with each other, and each output is a fourth of the input frequency. The 45 degree phase

7 Simulation Results

7.1 HFVCO

The HFVCO was simulated over process changes of 20% in resistance and capacitance and a 10% process variation in threshold voltage. It was operational with these variations over the desired frequency range of 87.9 - 107.9 MHz. Figure 9 is a plot of the spectrum of the output. The entire tuning range is 87 - 145 MHz over a control voltage of 0.5 - 3.5 V, which gives a sensitivity of about 21 kHz/mV. Over the FM broadcast band the sensitivity is about 14 kHz/mV.

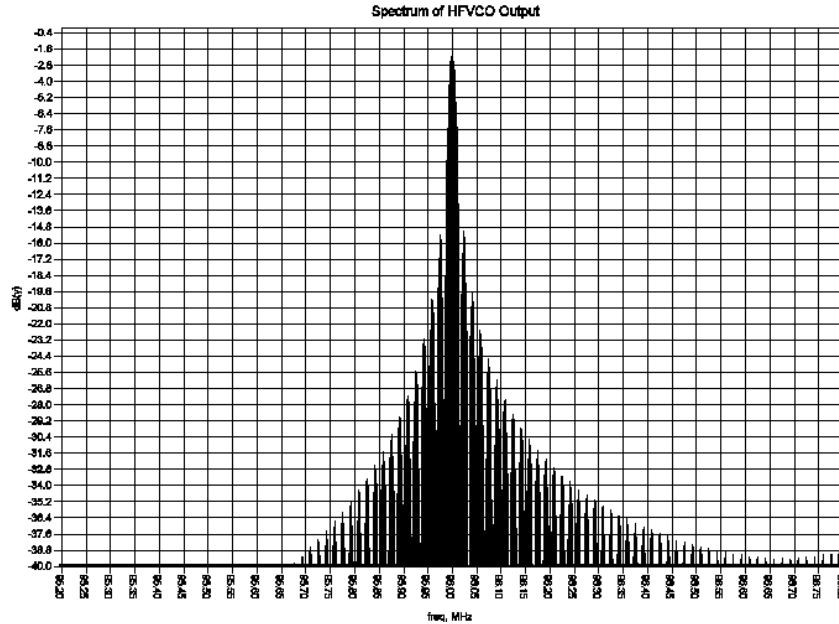


Figure 9: Spectrum of the HFVCO output

The output appears to have several harmonics present, but this is due to the way the spectrum was calculated. It was done by taking the Fourier series of the output of the HFVCO over a relatively short time period, therefore the spectrum appears as the Fourier series of a waveform that is sinusoidal during the duration of the simulation and zero at times other than this.

7.2 Image Reject Mixer

The image reject mixer was likewise simulated with a 20% variation in capacitor values and 10% variation in threshold voltages. Figure 10 is one end of the mixer output which shows a 1.2V peak-to-peak signal.

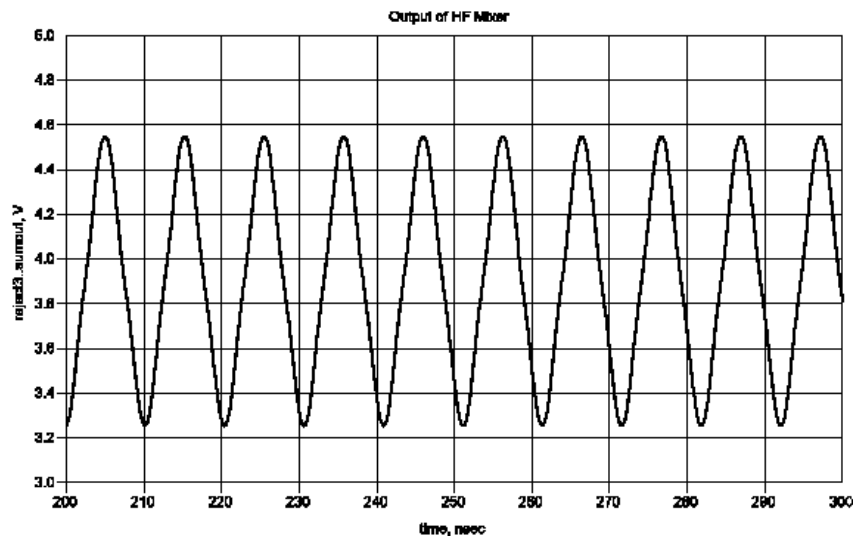


Figure 10: Output of the image reject mixer

The spectrum seen in Figure 11 shows that the 97.3 MHz signal is passed while the 97.9 MHz signal has been rejected. There is also a component present at 98.5 MHz that is 10 dB below the desired signal.

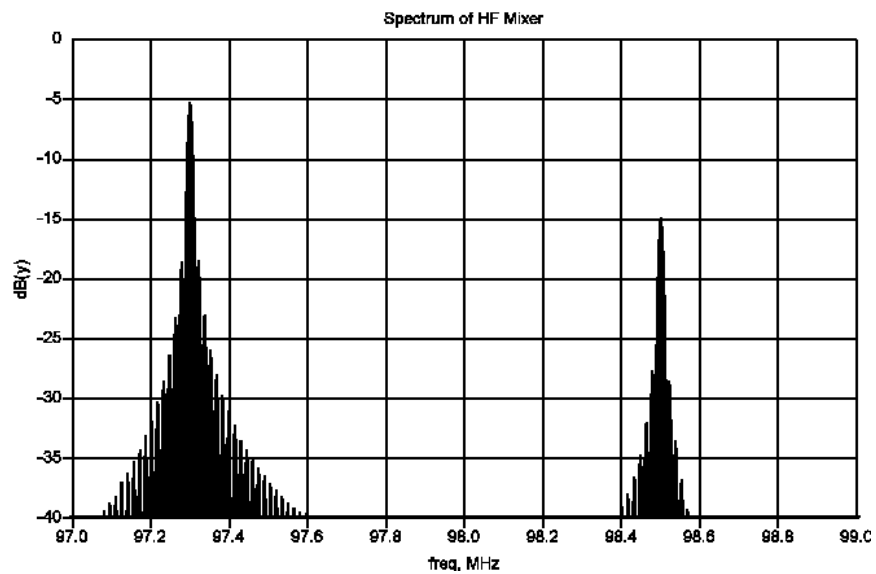


Figure 11: Spectrum of the image reject mixer output

8 Conclusions

The chips designed in the IC Design course performed better than expected, especially the Beta-Tronix chip. One drawback to the chips was that they were difficult to test. In future offerings of the IC Design course adequate testing plans should be made to speed up the testing process. Internal probe points should be used at all bias points to allow the entire system to be explored and to conserve the number of input and output pins needed.

VLSI ASIC Development course objectives 1, 2, 3 and 5 (see section 2) were met in the time allotted for the course, but objective 4 could not be completed by one student in this course offering. A sixteen week format would be a more realistic timeframe for a project of this size, and the possibility of having a small group of students in this class instead of one student could increase the breadth of the project.

Moving a college course beyond the standard lecture and test format can present excellent opportunities for learning. The continuation of the IC Design project in an independent study environment was very beneficial to both the professor and the student. The professor can get assistance from the student in evaluating the previous class project and course offering, while the student can gain valuable experience in aspects of VLSI ASIC development such as becoming more familiar with lab equipment, layout and simulation tools as well as expanding their circuit design portfolio. In this regard, all the benefits of this course were gained despite not all of the original objectives being met.