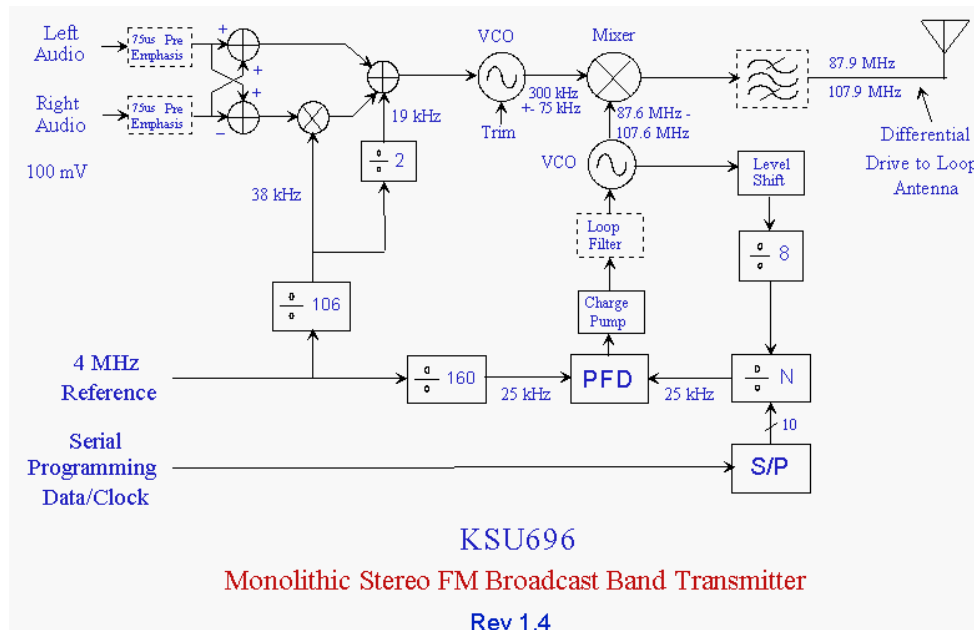


Monolithic Stereo FM Broadcast Band Transmitter
EECE 696 – Integrated Circuit Design
Kansas State University
Dr. William B. Kuhn

Beta-Tronix Testing Results for MOSIS
 by Matthew C. Peterson and Shobak R. Kythakyapuzha

Project Description

The class was divided into two companies: Alpha-Bits Semiconductors and Beta-Tronix. This report is for the Beta-Tronix design. Each company was responsible for the design, simulation and layout of a prototype of the product. Two different prototypes were sent to MOSIS for fabrication, and the testing of each prototype is described in this report. Design and layout information for this chip may be found on our web page at <http://www.eece.ksu.edu/~eece696/beta/beta.htm>. Included in this web page are operation and design descriptions, detailed schematics, simulation results and layout images.



Design Overview

The product is a prototype of a monolithic stereo FM broadcast band transmitter. The AMI ABN 1.5µm scalable CMOS process was used with a lambda of 0.6µm.

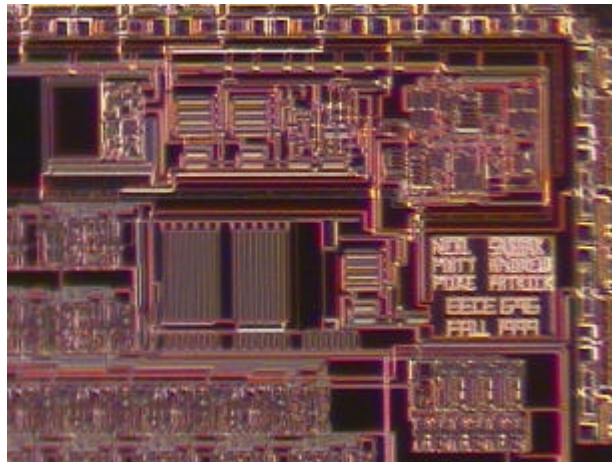
The input to the chip is a stereo audio signal approximately 100mV in amplitude, that has been preemphasized and is AC coupled to the input pins. To enable stereo transmission, a matrix of two-input summing amplifiers is used to create a left-plus-right channel and a left-minus-right channel. The left-minus-right signal is upconverted to a center frequency of 38kHz. The resulting signal is fed into a three-input summing amplifier along with the left-plus-right signal and a 19kHz-clock signal (which is used as a pilot tone in demodulation). The 38kHz clock is created from passing a 4MHz reference clock signal

(located off-chip) through a divide-by-106 counter. Passing the 38kHz clock through a divide-by-2 counter creates the 19kHz clock.

The output of the three-input summing amplifier is fed through a low frequency voltage-controlled oscillator (LFVCO) with a center frequency of 300kHz. The LFVCO varies between 225 and 375kHz, creating a 150kHz channel.

The output of the LFVCO is fed into a mixer along with an output from the high-frequency VCO (HFVCO). The mixer upconverts the output of the LFVCO to the broadcast band of 87.6MHz to 107.6MHz. The HFVCO is part of a phase locked loop (PLL). To start the PLL the output of the HFVCO is sent through a level-shifter. The output of the level shifter is passed through a divide-by-eight counter. The signal is then passed through a divide-by-N counter, which divides the signal so that the output has a center frequency of 25kHz. The serial programming data, which comes from an off-chip source, determines the number N. This data is fed into a 10-bit serial-to-parallel converter, which is input into the divide-by-N counter. This data determines the center frequency of the broadcast band.

The output of the divide-by-N counter is one of the inputs into a phase-frequency detector (PFD). The other input to the PFD is the output of a divide-by-160 counter. The input to the divide-by-160 counter is a 4MHz frequency reference located off-chip. The PFD compares the phase of the output of the divide-by-106 and divide-by-N counters and sends their difference to a charge pump. The output of the charge pump is then passed through a loop filter (located off-chip) and into the input of the HFVCO, completing the PLL.



Close-up of the Beta-Tronix Chip

Simulation and Layout Information

This design was simulated with Spice3f5 using the BSIM3 version 3.1 models at the four process corners over a temperature range of -20°C to 70°C . The layout was performed with Magic version 6.4.4 and converted to CIF format for submission to MOSIS.

Test Equipment

A Wavetek 810 was used for signal generation and clock references. A Hewlett-Packard 6236B was used for the power supply and trim voltages. The DC levels were measured with a Hewlett-Packard 3466A digital multimeter. A Fluke PM3392A oscilloscope was used for measurement of all analog and digital signals.

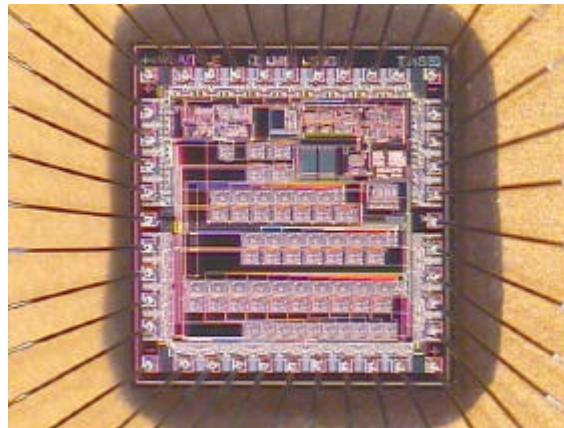
Beta-Tronix's Test Results

Summing Amplifiers and Low Frequency Mixers

The first test point was taken at the output of the LF mixer, which mixes the output of the left-minus-right summing amplifier with a 38kHz clock signal. For a 500mV input to the left channel and no input to the right channel, the mixer outputs 500mV as expected. When 500mV is input to the right channel and 500mV to the left channel, nothing is output from the mixer since this is the left minus right channel. When 440mV is input to the left channel and 220mV is input to the right channel, 220mV is output from the summer as expected. All of these test signals are 1kHz.

When there is no input to the left and right channels, and 2MHz is put on the clock input (a 4 MHz source was not available at the time) and a high signal is put on the clear pin, a 19 kHz signal is output from the two input summer. This indicates that the divide-by-106 counter is operating correctly.

With signals input into the left channel and a 2MHz signal on the clock pin, the output of the three input summer contained the input signal mixed with a 19 kHz signal, verifying correct operation of the LF mixer and the three-input summing amplifier. Without any input to the left or right channels there is no 9.5kHz signal observed, only a 19kHz signal from the divide-by-106 counter. This is due to the divide-by-2 counter not being connected correctly in the layout. Instead of Q' being connected to D on the D-flip-flop, Q was connected to D. This caused the output to remain latched to either high or low.



Beta-Tronix's Chip

D igital

The divide-by-106 counter outputs 19kHz for a 2MHz clock input and a high signal applied to the clear pin, so the divide-by-106 operation is performing correctly. The divide-by-160 counter outputs 12.5kHz for a 2MHz clock input and a high signal applied to the clear pin and so it is also performing correctly. The output square waves are sharp with adequately fast rise and fall times. The static flip-flops perform correctly up to a frequency of 70MHz which was within 30% of the simulated 100 MHz maximum toggle frequency.

Testing of the dynamic flip-flops was less successful. Even with a good square wave output from the level shifter in the PLL, the divide-by-eight counter did not produce an intelligible output.

LFVCO

With no trim voltage input, the LFVCO output a 435kHz square wave. As the trim voltage was increased, the frequency of the output decreased. For a trim voltage of 0.5V, a center frequency of 300kHz was output which was the desired frequency output. For an input sinusoid of 540mV peak-to-peak amplitude, the frequency changed by 666kHz, or about 1.2Hz/mV frequency deviation.

HFVCO

With no external capacitors, the HFVCO output an 8MHz signal. This was much less than the desired range of 87.6MHz to 107.6MHz. As with company alpha's chip, a lack of internal probe points prevented debugging this problem. The common-mode feedback loop is working correctly, though.

Mixer

Due to problems with the HFVCO, the mixer could not be tested. (Company beta's design did not include the probe points on the output of the HFVCO that were present in company alpha's design.)

Conclusions

While most circuits are functional, the lack of internal test points prevents us from individually testing the divide-by-2 counter, divide-by-eight counter, low-frequency mixer, two and three-input summing amplifiers, phase-frequency detector and charge pump. Instead these circuits are tested in conjunction with other parts and so it becomes more difficult to pinpoint any problems in the circuit. More internal test points for bias points and current references would aid the testing of this chip. Since this lack of internal probe points limited the testing of this chip, future versions of this chip will include more test points. To aid in this, our university has purchased some Picoprobes for the internal test points.